

High Productive 3D Stacking Process NCF, “AK-400 series”

Makoto Sato

Protection Film R&D Dept.,
Electronics-related Materials Development Center,
R&D Headquarters

Kazutaka Honda

Packaging Solution Center,
Packaging Materials Business Sector,
Advanced Performance Materials Business Headquarters

1 Abstract

Non Conductive Film (NCF) is applied for 3D-package which consists of stacking of Through Silicon Via (TSV) memory with narrow bump pitch and narrow gap.¹⁾

NCF is a film type under-fill and useful for 3D-package because it is void-less and has less fillet. On the other hand, NCF has two tasks. One is low productivity and the other is the risk of high warpage after reflow process, making the molding process impossible. To improve these tasks, Mold Reflow Process is developed. Mold Reflow Process is a serial process which includes the first step of chip pre-bonding, the second step of resin over-molding and the last step of connection by pressure reflow furnace. High productivity and low warpage are expected by applying Mold Reflow Process.

2 Characteristics of the Product

- Improves productivity by using batch processing in the pressure reflow process.
- Suppresses warpage by performing molding processing before the pressure reflow process.

3 Background of the Development

In the current NCF process, chips are pressure bonded in a two-step process: the temporary pressure-bonding process where positioning is performed after pickup, and the actual pressure-bonding process that makes solder connections. Productivity improvements in these processes are needed, because of the low UPH (units per hour) value, which shows that the number of packages produced per hour is low (ranging from several dozens to several hundreds). One method for improving productivity is a reflow process that makes solder connections in a batch. In this reflow process, after the temporary pressure-bonding process, heat processing is performed at a sufficiently high temperature to melt solder (in a reflow furnace, etc.). However, compared to the current process, this reflow process degrades the reliability of connections because of non-pressurization.²⁾ In addition, with chip-on-wafer (CoW) mounting, if there is significant warpage after the reflow process, the next molding process cannot be performed. Therefore, we devised a mold reflow process in which the molding process is performed first, and then solder connections are made in a batch by using pressure reflow processing. This new mold reflow process simultaneously suppresses warpage and improves productivity.

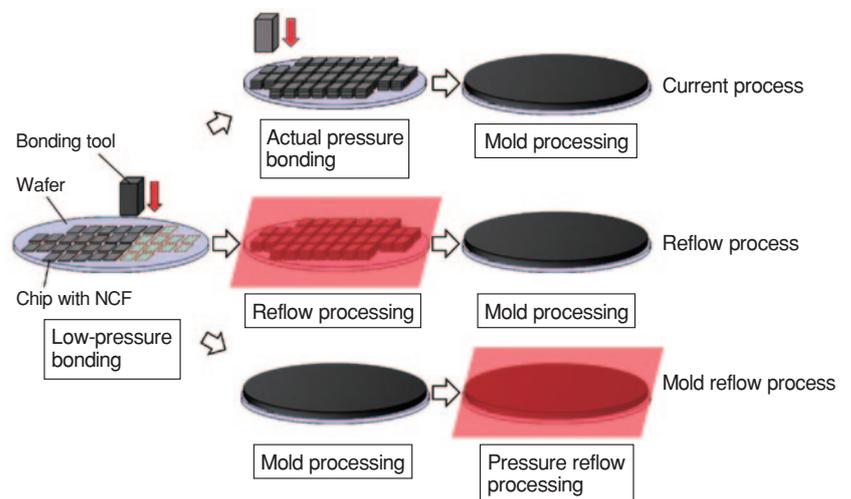


Figure 1 Assembly flow of each process

4 Technical Details

In the mold reflow process, solder connections are made by using reflow processing, which requires a reduction in the NCF viscosity. By increasing the resin fluidity in the temporary pressure-bonding process, we can achieve good solder connectability, as shown in **Figure 2**. In addition, we verified that reducing the viscosity (in comparison with the NCF used for the current process) could suppress the generation of voids.

We also measured the warpage of wafers after reflow processing for the following two cases: the case when molding was performed after the temporary pressure bonding of chips on wafers, and the case without such molding. **Figure 3** shows the measurement results. We verified that significant warpage occurs in the latter case (without molding), making it impossible to subsequently perform the mold process. We also verified that the former case (with molding in the mold reflow process) results in less wafer warpage than in the latter case (without such molding).³⁾

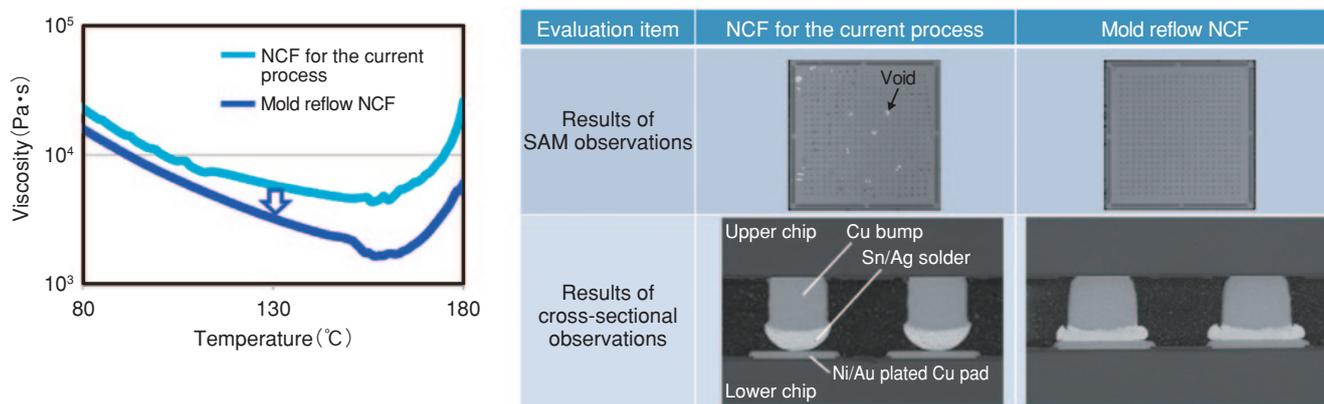
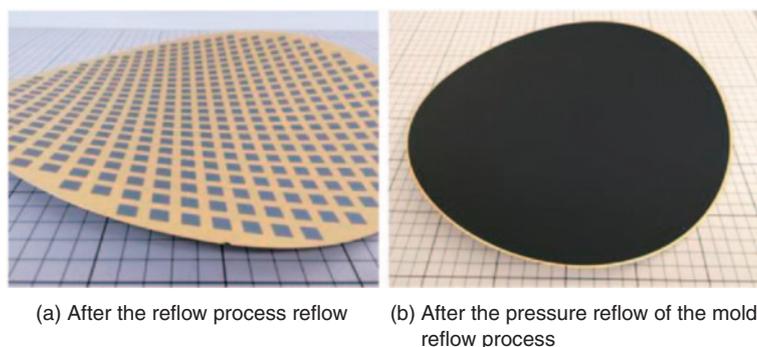


Figure 2 Measurement result of viscosity and void and connect-ability result after molding reflow process



#	Process	
①	Temporary pressure bonding	
②	Reflow process	After reflow processing
③		After mold processing
②'	Mold reflow process	After molding
③'		After pressure reflow processing

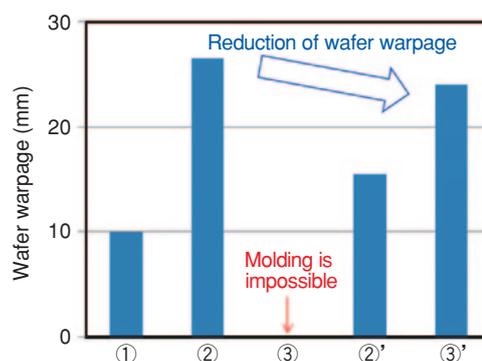


Figure 3 Comparison of warpage with and without molding process

5 Future Business Development

- Optimization of compositions to match the mounting process

[References]

- 1) Kazutaka Honda, Tetsuya Enomoto et al., “NCF for Wafer Lamination Process in Higher Density Electronic Packages”, Proceedings of 2010 Electronic Components & Technology Conference
- 2) Hitoshi Onozeki, Hiroshi Takahashi et al., “In plane collective

CoS assembly by NCF-TCB enabled using the newly developed bonding force leveling film”, proceeding of 2016 Electronic Components & Technology Conference

- 3) Kazutaka Honda, Hirokazu Noma et al., 2017 IEEE 67th Electronic Components and Technology Conference, pp.719–724