

# Hitachi Chemical Technical Report

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**Hitachi Chemical**  
Working On Wonders



**HITACHI**

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(Background) Floor entrance



(Upper right) Building entrance



(Lower left) Clean room



(Lower right) Yellow room

(Cover picture) the semiconductor Jisso open laboratory



Vice President and Executive Officer  
General Manager  
Advanced Performance Materials Business  
Headquarters

Hiroyuki Yamashita

# Initiative for a Total Solution that Realizes the Customer's Idea and Contributes to the Development of Society

## 1. Changes in social and market trends, and future expectations

The world is on the brink of a new era, which is marked by an increase in the amount of information recorded and accumulated about our daily consumption and work. By organizing this information, we are increasingly able to identify and resolve new problems. Based on these trends, we can expect that, in the future, never-before-seen services will be available and will contribute significantly to society.

Until now, various convenient services have been developed through the use of personal computers, mobile phones, and smartphones. This evolution in services is supported by information and communication technology, which is advancing very fast. Applications of this technology are not limited to the fields of information networks and cloud environments, but have expanded into the field of automobiles, industrial robots, and medicine, allowing new services to be created in wide industries. This trend is only just beginning and is expected to continue for a long time.


## 2. Hitachi Chemical's beginnings and our contribution to the development of new industries

In the late 1940s, Bell Laboratories invented the point-contact transistor. This was followed by the invention of the integrated circuit (IC) in the latter half of the 1950s. These developments led to the rapid growth of the semiconductor industry all around the world, bringing new prosperity to people's lives.

Hitachi, Ltd. was established in 1912 and now more than 50 years passes since establishment of Hitachi Chemical as an independent entity separate from Hitachi, Ltd. in 1962; we have produced insulating varnishes for motors, industrial laminates for PWB, porcelain insulators, and carbon brushes. We also expanded upon these products to create many new products through R&D and manufacturing. Throughout our company's history, we have created many products that support the current ICT industry, such as CMP slurries used to form circuits on semiconductor wafers, die attach film used to protect and fix wafers on which circuits have been formed, and epoxy molding compounds for semiconductors and package substrates. The materials, processes, and evaluation techniques that we have cultivated along the way continue to contribute to the high integration and miniaturization of semiconductors even today.

## 3. Total solutions to help customers realize their ideas

The mission of the Hitachi Chemical Group is to contribute to society through the development of superior technologies and products. Our company aims to achieve sustainable growth by resolving new social issues and by continuing to provide new value to society. We believe that the key to accomplishing this is information. For example, we



consider information (such as information on global climate change, market and consumer trends, global distribution and transportation networks, and the health management and productivity of employees) to be the starting point for identifying and understanding social issues. If we can create a mechanism for collecting, managing, and analyzing such information—a mechanism that leads to risk mitigation and issue resolution—we believe that businesses can contribute to the advancement of society. As you know, the development of next-generation technologies for wireless communication (such as IoT and 5G technology) has brought about significant changes in the processes of information collection, management, and analysis. For these technologies to be broadly adopted by society, extensive software programs are required, in addition to semiconductor devices and other hardware. Other key factors are how to combine hardware and software, how to design complex systems to make them user friendly, and how to link these systems to excellent services in a timely manner.

In particular, when working on a development project in a customer, it is imperative that customers not only assemble specific hardware devices, but also build advanced software and systems and create products and services of superior design before any of competitors. As a result, such development projects require larger budgets and more labor hours, due to the increasing number of products to be developed and the increasing complexity of process management with respect to the mounting of semiconductors. In actuality, even if a customer comes up with an idea for a product they want or something they want to try out within the allotted time or budget, oftentimes the idea cannot be acted on immediately.

When a customer wants to carry out an idea, in addition to having an understanding of the customer's actual development site, we must also (1) clearly define the required tasks, (2) have access to the necessary technology, and (3) have somewhere to conduct the necessary studies. Furthermore, we must put forth proposals for total solutions that resolve issues at the customer's development site and that can be feasibly accomplished within a short period. These proposals should make use of our proprietary processes, parts, and materials technologies, and can include collaborative efforts with other companies that have outstanding technologies.

This issue of *Hitachi Chemical Technical Report* introduces in detail our efforts in relation to the above and aims to give all of our stakeholders an idea of Hitachi Chemical's future business development.

#### 4. Future prospects

As was stated earlier, our mission is to provide new value that is ahead of the times, and to contribute to the advancement of society. Going forward, the Hitachi Chemical Group will collectively work toward growth as a corporate group that contributes to society under the Hitachi Founding Spirit, which values pioneering spirit, sincerity, and harmony. To this end, we will effectively deploy our management resources worldwide; implement management that allows us to resolve issues spanning multiple business areas; foster professional human resources; and build a network of knowledge that goes beyond the scope of our company.



# Action for a Total Solution that Reinforces the Packaging Materials Business

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In recent years, advances have been made with respect to information and communications systems (most notably, 5G technology), marking the coming of the era of IoT (Internet of Things), where everything is connected to the internet. At the same time, there are limitations in increasing the density of semiconductors, and the semiconductor packages mounted in electronic devices used in various environments are required to have a more complicated structure (such as three-dimensional Jisso) and higher reliability.

We have relocated the open laboratory established in Tsukuba in 2014 to Kawasaki City, where it is now called the “New Open Laboratory”. At the New Open Laboratory, not only do we propose conventional total solutions for material combination and processing, but we also promote open innovation projects that center on the laboratory and that are carried out with the cooperation of other companies and organizations. Through open innovation, the laboratory accelerates the realization of next-generation semiconductor packages. In this paper, we introduce some of the new innovations and activities of the New Open Laboratory.

## 1

## Introduction

The sudden high functionality of information terminal electronic apparatus represented by smartphones and tablet PCs in recent years is accelerating the rapid miniaturization and high densification of packages. Therefore, the structure is more complicated as shown not only by the high densification of surface mounting but also by the realizations of three-dimensional package with devices having penetration vias and by the fan-out wafer level package (hereafter referred to as FO-WLP) that enabled high density Jisso in Jisso process by rewiring technology, and the Jisso process is also diversified.

On the other hand, since the product cycle is shortened, in order to realize such complicated package in a short period of time, it is important not only to timely propose new Jisso materials but also to speedily propose a total solution from the viewpoint of customers, including the Jisso process and material combination.

In 1994, Hitachi Chemical Co., Ltd. established the Jisso Center for the purpose of performing the evaluation and analysis of semiconductor Jisso materials by ourselves first in the world and has promoted developing various types of Jisso materials. Thus, we are enlarging the product lineup from the frontend to the backend.

In June 2014, in order to deal with large changes in the above-mentioned package structures and Jisso processes, we renewed the Jisso and evaluation facilities in the Jisso Center and established the semiconductor Jisso open laboratory (hereafter referred to as the “Open Laboratory”) based on a variety of Jisso material technologies, Jisso evaluation and analysis technologies. The Open Laboratory enabled the Jisso and evaluation of various advanced packages of the customers using various material lineups including our new materials.

In addition, using the Open Laboratory as a core base, we are promoting construction of new materials and processes positively in cooperation with manufacturers of equipment, processes, and components. Furthermore, using abundant material data bases accumulated, we perform various simulations to deal with the customer’s next generation package structure that is still in the design phase, and we promote the proposals of the optimum material combination, the productivity improvement of the customers, and the new processes contributing to suppressing new investment.

## 2 Expansion and Relocation of Open Laboratory to Shin-Kawasaki District

During four years since the establishment, the customers from 600 or more companies visited the Laboratory. We developed materials using the above-mentioned scheme in cooperation with these customers and acquired the approval of about 90 of new materials through the proposal of total solutions and through the activities that shorten the customer's approval period. Thus, our Semiconductor Jisso Open Laboratory has contributed to our business. However, since there were major problems concerning geographic inconvenience for overseas customers and the limitation of functional expandability due to restrictions on space, we enlarged the size to about three times to complete the relocation to Shin-Kawasaki District, Kawasaki, Kanagawa. The features and outline of the new Open Laboratory are shown below:



Appearance of building



Building entrance



Floor entrance



Office area

### (1) Wafer process and assembly areas

In the wafer process and assembly areas, we installed a stealth laser dicer manufactured by DISCO Corporation in addition to the conventional blade dicer. The new dicer is used for processing ultrathin wafers of 50  $\mu\text{m}$  or less, and high efficiency of evaluation is expected by the processing time reduction using device wafers and the improvement of yield by crack reduction.

A new type of die bonder manufactured by Fasford Technology Co., Ltd. was installed for the die bond process. This bonder is used for high speed continuous bonding because the improvement of UPH of 20% as the ratio to the conventional machine enabling the evaluation in the reproduced process environment of customer's mass production machine concerning the thermal history of materials and circuit boards. Furthermore, since the bonder is provided with bonding accuracy as high as 10  $\mu\text{m}$  and a micro crack detection function, higher evaluation efficiency, package assembly integrity, and improvement of evaluation accuracy are expected.

The existing facilities also realized the functional improvement by renewal to a new type of machine. We will flexibly and quickly deal with diversified customer's processes by realizing improvements in processing quality by installing a new type of blade dicer with enhanced detergency, installing a dicer capable of processing large-size circuit boards in sizes up to 600 mm  $\times$  600 mm considering panel process, and constructing a pure water circulating system to be used for them.



Wafer process area



Assembly area

## (2) Advanced process evaluation area

FO-WLP has attracted attention in recent years because it can realize the miniaturization, thinning and its high frequency characteristic by shorter wiring length. FO-WLP has various construction methods, which can be basically classified into two methods. The die first method that forms re-distributed layer (RDL) for fan-out on semiconductor devices and the RDL first method that mounts semiconductor devices on the previously formed RDL. Our Open Laboratory in Shin-Kawasaki can implement both diversified construction methods, and the trial manufacturing line capable of processing from the wafer level to the panel level (fan-out panel-level-package: hereafter referred to as FO-PLP) was constructed in this laboratory. The processes for fan-out package mainly consist of the RDL forming process, encapsulant molding process, carrier debonding process, and chip mounting process. The Shin-Kawasaki site has a group of facilities capable of performing a series of processes from the 12" wafer carrier size to the maximum 510 mm × 515 mm size panel and can evaluate various materials and processes related to fan-out packages.



Advanced process evaluation area

The RDL forming process is applied to a series of processes, such as the liquid material coating for applying and forming RDL insulation materials, film material lamination, exposure and development of photosensitive materials, seed metal sputtering, plating resist forming, Cu electroplating forming, resist stripping, and seed metal etching. In particular, we installed a stepper exposure machine (Sc6k manufactured by Cerna Precision, Inc.) with high resolution of the minimum line / space = 2 μm / 2 μm to handle the above large-size panel to enable application to further high densification RDL in the future.

Concerning the encapsulant molding process, we installed a new compression molding machine (CPM1180-S manufactured by TOWA CORPORATION) to manufacture the maximum 320 mm × 320 mm size circuit boards at the Tsukuba site, thus enabling the manufacture of up to 510 mm × 515 mm size boards. Similarly concerning the sputtering process, we installed a new sputtering facility (SIV-500 manufactured by ULVAC, Inc) to manufacture the same size boards.

Concerning the die mounting process, the Tsukuba site applied flip chip bonding (FCB) to panels of the circuit board in sizes up to 300 mm × 300 mm, and the Shin-Kawasaki site installed a new flip chip bonder (MD4000 manufactured by Toray Engineering Co., Ltd.) capable of manufacturing the maximum 600 mm × 600 mm size boards, a new flip chip bonder (FC3000W manufactured by Toray Engineering Co., Ltd.) with loading accuracy of ±2 μm and loading ability of the maximum 1,600 UPH, and a die mounter (NXT-Hw manufactured by FUJI Corporation) with mounting accuracy of ±8 μm and loading ability of 4,000 UPH to match panel enlargement and higher accuracy mounting in the future.

## (3) Photosensitive material evaluation area (yellow room)

In order to construct a micro wiring forming line to be essential for next generation packaging technology realizing higher densification, the yellow room area can now deal with up to 600 mm × 600 mm from the conventional 12" wafer size by installing a slit coater, a vacuum laminator, and a exposure machine. In addition, the new installation of the above-mentioned stepper



exposure machine Sc6k manufactured by Cerma Precision, Inc. in the newly established clean room of Class 100 allowed us to expect the realization of stable micro pattern processing of  $L / S = 2 / 2 \mu\text{m}$ . In addition, the installation of large-size sputtering equipment and plating-related facilities enabled Cu wiring forming on various substrates.

We constructed the evaluation line leading to the micro wiring forming using photosensitive materials, the application to the next-generation Cu wiring plating, and the promotion of applied material and process development by concentrating these facilities in the above clean room.



Yellow room

#### (4) Evaluation and analysis area

We newly installed an advanced evaluation facility to improve the accuracy of analysis in the minute region and increase the speed of failure analysis. We installed a field emission type of scanning electron microscope (FE-SEM) capable of magnifying up to 2 million times and a high-performance focused ion beam (FIB) capable of high-speed and large area processing using a high current beam of 90 nA, thus having constructed assemble method evaluation and precision analysis lines concerning micro wiring of  $L / S = 2 / 2 \mu\text{m}$  or less. We installed an ultrasonic flaw detector, a semi-automatic prober, and a laser displacement gage as evaluation and analysis equipment for FO-PLP of which adoption is hereafter expected to increase. All the equipment has an inspection range of  $600 \text{ mm} \times 600 \text{ mm}$  or more of which utilization enabled the identification of problem occurrence timing during forming of the rewiring layer and the measurement of warpage after encapsulation while keeping the panel size as it is. Furthermore, the correction of warpage by an ultrasonic flaw detector with a water flow adsorption stage enabled non-destructive visual inspection of voids and deramination.



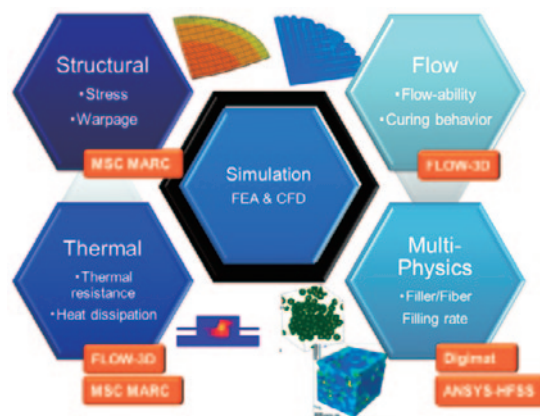
Evaluation and analysis area

#### (5) Simulation area

The Open Laboratory have performed analyses of warpage and stress, fatigue life analysis, and heat dissipation analysis using non-linear structure simulation (Marc: MSC Software Corporation) by fully utilizing abundant material databases accumulated by Hitachi Chemical Co., Ltd. to support material development. Since the utilization of CAE (computer aided engineering) has progressed in recent years, we newly installed a flow simulator (Flow3D: Flow Science Japan), a composite material simulator (Digimat: MSC Software Corporation), and an electromagnetic field simulator (Ansys HFSS: Ansys Japan). In flow analysis, the resin that flows inside a mold chase while causing the curing reaction and the pressure bonding behavior of film-like materials can be analyzed. In addition, in composite material analysis, composite materials that were conventionally handled as an integral



Simulation area



Capability of simulation



part can be analyzed by dividing into individual components, and the reproduction of stress of the microstructure and accurate property generation of material having anisotropy and the reverse engineering in which microscopic structure is estimated from macroscopic properties of composite materials can be performed. In electromagnetic analysis, the effects of relative dielectric constant and dielectric loss tangent of materials affecting radiation and the eye pattern of circuits can be analyzed. Shin-Kawasaki aims to contribute to the promotion of high-level material development by fusing these analysis technologies.

## (6) Fukuoka IST (Fukuoka Industry, Science & Technology Foundation) area

In the relocation to Shin-Kawasaki this time, we are promoting the construction of a trial manufacturing system to respond to large-size FO-PLP. However, it was difficult to relocate the large-size plating facility and the etching facility necessary for rewiring forming because there were issues of large amounts of chemicals, waste liquid treatment, and space. Therefore, we newly installed plasma equipment (AP-1500: Nordson Corporation), stripping equipment (ASEP-S600: Japan Create Co.,Ltd) and etching equipment (SEP-S600: Japan Create Co.,Ltd) in Research Center for Three-Dimensional Semiconductors (Fukuoka IST, Fukuoka) having excellent technologies for three-dimensional Jisso and circuit boards with built-in parts, and constructed the rewiring forming line applicable to 510 mm × 515 mm size. Thus, fine rewiring ( $L / S = 2 / 2 \mu\text{m}$ ) forming responding to the large-size with various material combination can be implemented. In addition, the utilization of knowledge in the Fukuoka IST enables the expectation of a synergistic effect in the development of new processes.



Research Center for Three-Dimensional Semiconductors



Batch type stripping equipment

## 3 Consortium JOINT

In June last year, the consortium JOINT: (Jisso Open Innovation Network of Tops) consisting of 17 companies involved in the development of semiconductor Jisso materials and equipment was established, and activities were started using our semiconductor Jisso open laboratory as a base. This consortium contributes to reductions in labor and time of the customer in the speedy development of packages by providing the customers of semiconductor manufacturers with total solutions, including from the development of advanced Jisso technology to Jisso processes using materials and equipment owned by participating companies.

In recent years, as the utilization of artificial intelligence (AI) and IoT that connects everything to the Internet and the market of automatic operation and electric vehicles (EV) are expanding, high performance sensors, radio terminals, and base stations enabling high speed data communication, and servers and data centers capable of processing huge amount of information at high speed, are highly required. Since this circumstance diversified the functions required for semiconductors loaded to various appliances and their structure is more and more complicated, larger numbers of materials and devices are now used for manufacturing packages. Therefore, there were problems where a lot of work and time are required when the customers develop packages because the customers must procure materials and equipment from many supplying companies and evaluate them individually.

Considering this situation, Hitachi Chemical Co., Ltd. established the consortium JOINT where semiconductor Jisso technology is developed in order to quickly provide customers with a comprehensive one-stop solution by combining various materials and processes. Although the conventional semiconductor Jisso open laboratory was based on a cooperation system of one-to-one, namely Hitachi Chemical Co., Ltd. and an equipment manufacturer or Hitachi Chemical Co., Ltd. and a material manufacturer,

JOINT can mutually utilize technology and information between Hitachi Chemical Co., Ltd. and multiple enterprises depending on the development theme.

Specifically, it is now possible to quickly provide customers with total solutions, such as the optimum combinations of various materials and processes required for manufacturing of packages and new packages. In addition, since the combination of such materials and equipment enables the evaluation of materials and equipment in the condition close to that of semiconductor evaluation test conducted by the customer, the labor for evaluation individually performed by the customer for each supplier can be omitted. This enables the contribution to the reduction of labor and time in the development of packages for which the speed is essential.



Logo of consortium JOINT



Office dedicated to consortium members

## 4 Future Business Development

Hitachi Chemical Co., Ltd. will continuously approach the creation of new products and new businesses in the high-end field by further polishing a variety of our advantageous technical abilities. We will assume the relocated and functionally enhanced Open Laboratory as the strategic base for the Jisso material business, approach the promotion of further open innovation together with the customers and the consortium-participating cooperative companies as one-stop solution provider in addition to providing various materials, and contribute to the realization of new advanced packages.

# High Productivity Technology for Semiconductor Process

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## 1 Abstract

WLP applications such as FO-WLP and FI-WLP are expanding recently from the viewpoint of miniaturization and electrical characteristics of semiconductor PKGs.<sup>1)</sup> This assembly is conventionally conducted by one-by-one die replacement process after dicing for die gap widening by using die-mounter. As miniaturizing and thinning of the die, the issues of time-consuming step to replace die one-by-one and the die crack have been revealed.<sup>2)</sup> To solve the issues, we developed a high productivity process that does not require die replacement and a new expanded film essential to the process.<sup>3)</sup> This process consists of the expanding step of the film on which diced-wafer is mounted and the transferring step of the all dies to the carrier simultaneously. Therefore, the new process doesn't need the time-consuming die replacement. In this report, we discuss the development of the expanding film and a series of the processes.

## 2 Characteristics of the Product

- Highly adhesive film that has high expandability for significantly expanding the die gap without causing die peeling.
- Process that enables high productivity by eliminating the need for die re-placement.

## 3 Background of the Development

Because die have become smaller and thinner, die cracks occur during the WLP assembly process. The side protection process, which covers the periphery of the die with encapsulating material, is the most common solution to this problem. The general flow of processes for this solution is as follows: (1) dice the wafer; (2) re-place the die on the carrier by using a die mounter that widens the die gap; (3) perform overmolding; (4) dice the molding material after peeling the carrier. However, as die become smaller, the number of die increases as a result, and the process of re-placing die on the carrier requires a significantly greater amount of time. Therefore, we have developed a high-productivity process that does not require die re-placement (**Figure 1**), as well as a new expanding film.

## 4 Technical Details

The properties of the expanding film we developed are shown in **Table 1**. Measurements of the die gaps after expansion were obtained by measuring the points shown in **Figure 2**. The expanding film has higher peeling strength and higher expandability in comparison with the properties of conventional films. The initial die gap (after dicing) of approximately 0.05 mm can be widened to 1.5 mm after the film is expanded. In addition, the results of visual observation and die gap measurement after expanding and molding revealed that no die peeling or die shift occurred during the series of processes (**Figure 3**). Furthermore, it was verified that no die peeling or cracking of the molding material occurred even in the dicing process after molding. Thus, the series of processes using the expanding film was verified.



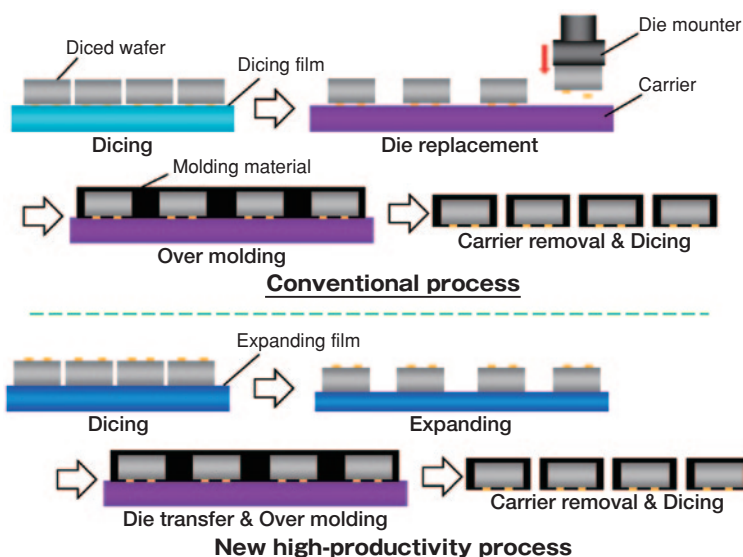


Figure 1 Conventional process and high productivity process flow with expanding film

Table 1 Properties of expanding film

Item		Unit	Conventional dicing film	Expanding film
Film thickness		μm	110	110
Peel strength*1	Before UV irradiation	N	1.0	6.0
	After UV irradiation	N	0.2	0.2
Die gap after expanding*2*3		mm	< 0.1	Up to 1.5

\* 1) Peel strength width: 25 mm

\* 2) Evaluated size: 8 inch wafer, die size 5 mm × 5 mm

\* 3) Expanding condition: Temp 50°C

Thrust-up speed 5 mm/s

Thrust-up height 100 mm

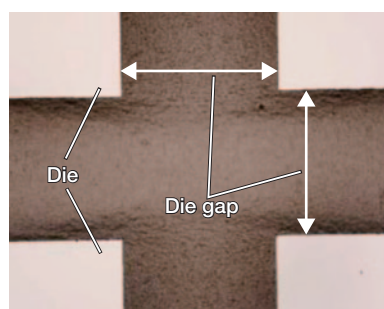


Figure 2 Measurement points of die gap

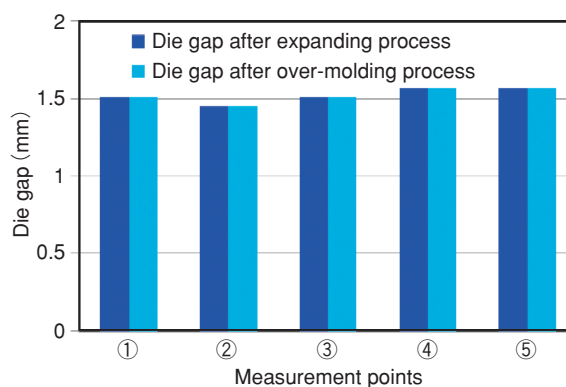
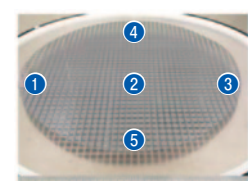
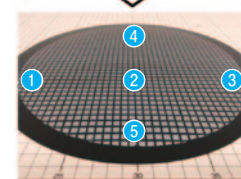


Figure 3 Die gap after each process



After expanding process



After over-molding process  
(After carrier removal)

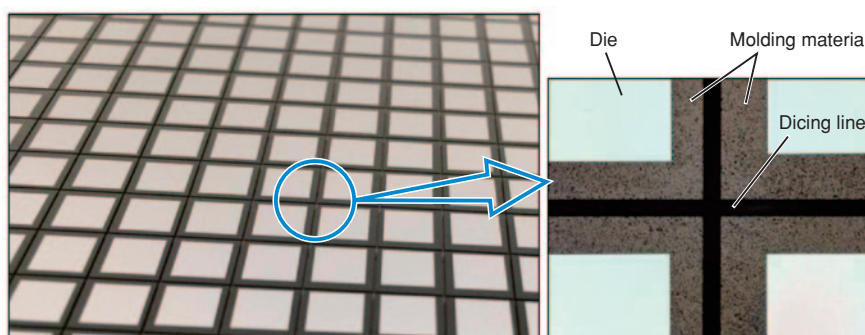


Figure 4 Molding material dicing

## 5 Future Business Development

- Deployment of this technique to FO-WLP and to micro LEDs (light emitting diodes)

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# High Productive 3D Stacking Process NCF, “AK-400 series”

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## 1 Abstract

Non Conductive Film (NCF) is applied for 3D-package which consists of stacking of Through Silicon Via (TSV) memory with narrow bump pitch and narrow gap.<sup>1)</sup>

NCF is a film type under-fill and useful for 3D-package because it is void-less and has less fillet. On the other hand, NCF has two tasks. One is low productivity and the other is the risk of high warpage after reflow process, making the molding process impossible. To improve these tasks, Mold Reflow Process is developed. Mold Reflow Process is a serial process which includes the first step of chip pre-bonding, the second step of resin over-molding and the last step of connection by pressure reflow furnace. High productivity and low warpage are expected by applying Mold Reflow Process.

## 2 Characteristics of the Product

- Improves productivity by using batch processing in the pressure reflow process.
- Suppresses warpage by performing molding processing before the pressure reflow process.

## 3 Background of the Development

In the current NCF process, chips are pressure bonded in a two-step process: the temporary pressure-bonding process where positioning is performed after pickup, and the actual pressure-bonding process that makes solder connections. Productivity improvements in these processes are needed, because of the low UPH (units per hour) value, which shows that the number of packages produced per hour is low (ranging from several dozens to several hundreds). One method for improving productivity is a reflow process that makes solder connections in a batch. In this reflow process, after the temporary pressure-bonding process, heat processing is performed at a sufficiently high temperature to melt solder (in a reflow furnace, etc.). However, compared to the current process, this reflow process degrades the reliability of connections because of non-pressurization.<sup>2)</sup> In addition, with chip-on-wafer (CoW) mounting, if there is significant warpage after the reflow process, the next molding process cannot be performed. Therefore, we devised a mold reflow process in which the molding process is performed first, and then solder connections are made in a batch by using pressure reflow processing. This new mold reflow process simultaneously suppresses warpage and improves productivity.

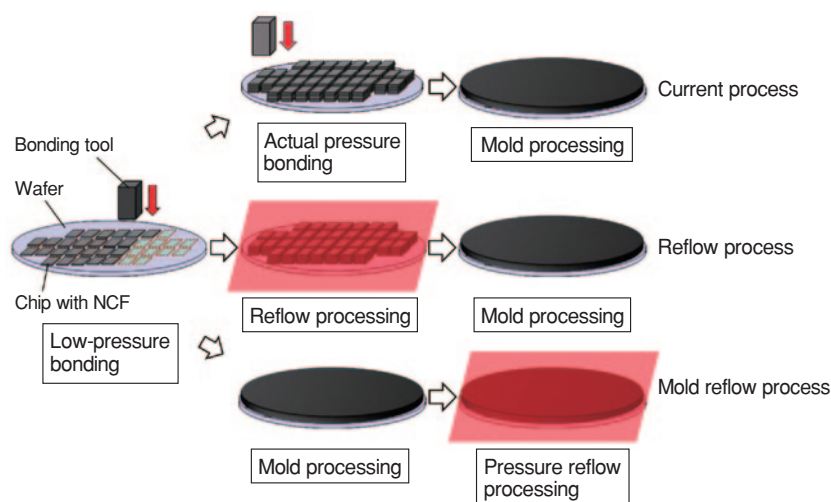


Figure 1 Assembly flow of each process

## 4 Technical Details

In the mold reflow process, solder connections are made by using reflow processing, which requires a reduction in the NCF viscosity. By increasing the resin fluidity in the temporary pressure-bonding process, we can achieve good solder connectability, as shown in **Figure 2**. In addition, we verified that reducing the viscosity (in comparison with the NCF used for the current process) could suppress the generation of voids.

We also measured the warpage of wafers after reflow processing for the following two cases: the case when molding was performed after the temporary pressure bonding of chips on wafers, and the case without such molding. **Figure 3** shows the measurement results. We verified that significant warpage occurs in the latter case (without molding), making it impossible to subsequently perform the mold process. We also verified that the former case (with molding in the mold reflow process) results in less wafer warpage than in the latter case (without such molding).<sup>3)</sup>

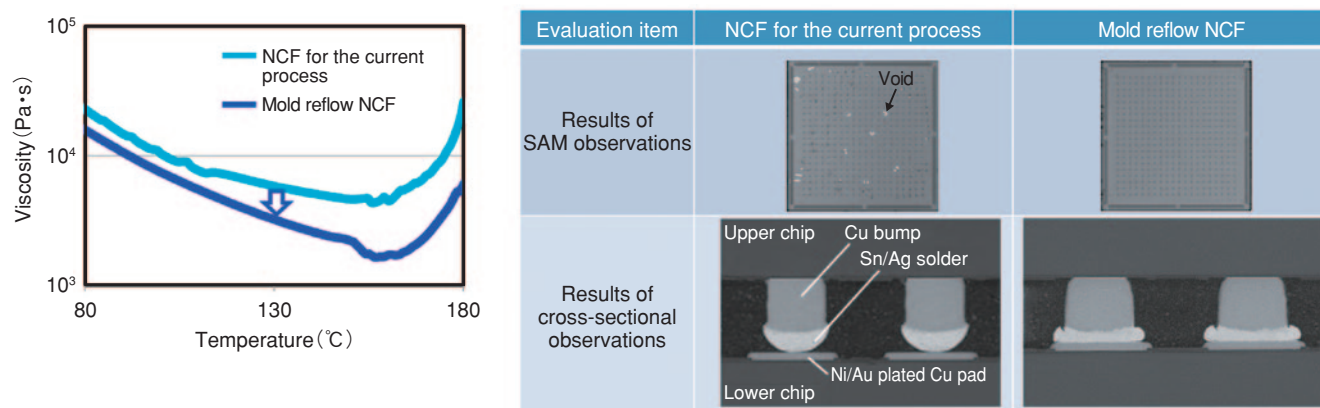
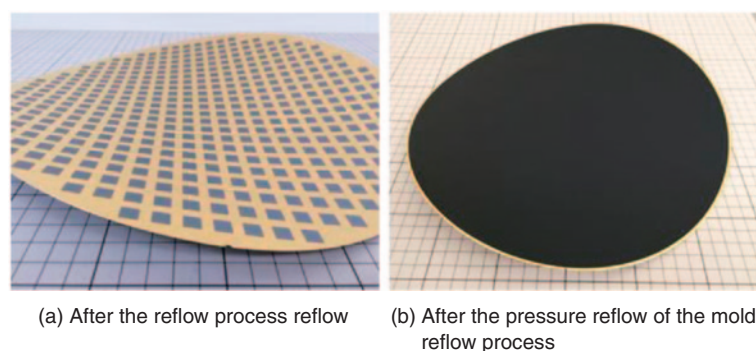


Figure 2 Measurement result of viscosity and void and connect-ability result after molding reflow process



#	Process	
①	Temporary pressure bonding	
②	Reflow process	After reflow processing
③		After mold processing
②'	Mold reflow process	After molding
③'		After pressure reflow processing

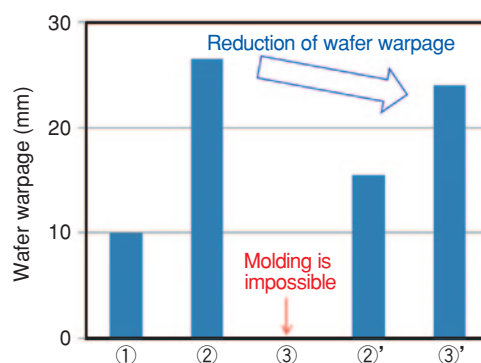


Figure 3 Comparison of warpage with and without molding process

## 5 Future Business Development

- Optimization of compositions to match the mounting process

### [References]

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- 2) Hitoshi Onozeki, Hiroshi Takahashi et al., "In plane collective

CoS assembly by NCF-TCB enabled using the newly developed bonding force leveling film", proceeding of 2016 Electronic Components & Technology Conference

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# Granule-Type Encapsulating Compound for Compression Molding

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## 1 Abstract

In recent years, studies have been conducted on compression molding because of its potential to reduce costs through the miniaturization and slimming down of semiconductor packages, and through batch molding (achieved via enlargement).

With compression molding, a powder-type encapsulating material is supplied directly into the mold cavity, decompressed, and then molded. As such, it is necessary to control the shape of the encapsulating material in order to prevent fluctuations in the resin thickness resulting from equipment contamination or from weight variation.

We have developed a method for producing a granule-type encapsulating compound that has a sharp particle-size distribution, and have also studied the compound's de-foaming property, which helps suppress resin leakage during decompression. By combining these technologies, we have developed a granule-type encapsulating compound for use in compression molding.

## 2 Characteristics of the Product

- Fine powder control reduces the contamination of equipment due to spraying powder and improves productivity.
- A uniform granule size improves the precision of package thickness.
- The introduction of de-foaming technology helps suppress resin leakage during molding.

## 3 Background of the Development

In recent years, studies have been conducted on compression molding for semi-conductor packages because of its potential to reduce costs through batch molding and its applicability to larger circuit boards and slimmer packages. With compression molding, a powder-type encapsulating material is used and resin is supplied directly into the mold cavity. As such, it is necessary to control the shape of the encapsulating material in order to prevent fluctuations in the resin thickness resulting from equipment contamination or from weight variation. To address this need, we developed a method for producing a granule-type encapsulating compound that has a sharp particle-size distribution. Another issue we needed to address was resin leakage caused by the foaming of the encapsulating compound during decompression and de-foaming, processes that are required for compression molding. To tackle this issue, we introduced foam-suppression technology to create a new encapsulating compound for compression molding.

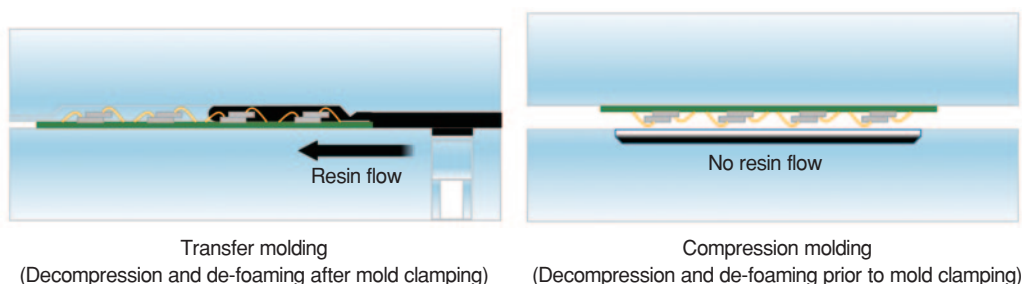


Figure 1 Method for encapsulating semiconductor packages

## 4 Technical Details

### 1. Method for producing a granule-type encapsulating compound

The fine powder in granule-type encapsulating compounds consist mainly of powder created during manufacturing and powder created as a result of the chipping and scraping that occurs during transport within equipment or during weighing by the vibration feeder. First, we studied the manufacturing methods and the conditions required to achieve a sharp particle-size distribution. As a result, we were able to control the granule particle-size distribution to between 0.4 mm and 1.2 mm, and to

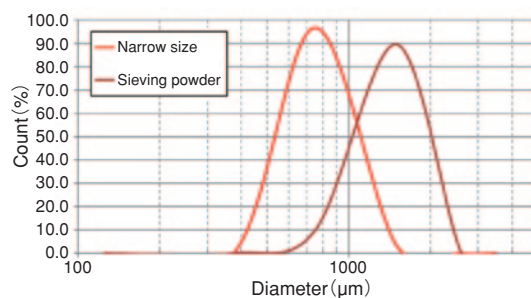
reduce chipping of the granules by improving the uniformity of the granule surface. We were able to verify that granules produced by using this method maintain stable dimensions and generated less fine powder.

## 2. Resin leakage

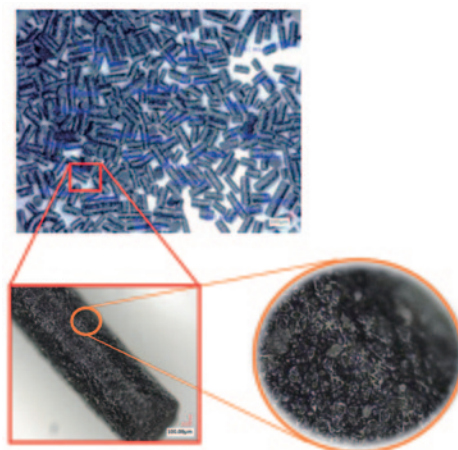
During decompression, gas trapped between the granule particles, and the volatile components of the encapsulating compound expand. This causes the compound to foam and its volume to increase, which in turn causes resin to leak from the mold.

In other words, to control resin leakage, we need to limit the amount of volatile components and to quickly remove trapped gas during decompression. Conventionally, resin leakage was suppressed by raising the melting point of the encapsulating compound, thereby allowing gas to escape from between the particles. However, an increased melting point sometimes led to wire deformation. Similarly, because the granule particles no longer melted easily, the external appearance of particle surfaces was poor.

Our new de-foaming technology rapidly breaks up foam that forms in the encapsulating compound, facilitating the release of trapped gas and volatile components and thus suppressing foaming and an increase in the volume of the encapsulating compound. The new material that we produced by using this method has been praised by customers for its low resin leakage and extremely low viscosity.

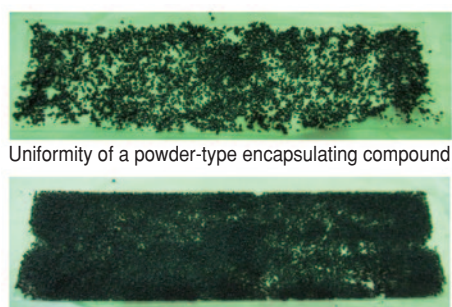


Comparison of the particle size distribution between granules and powder

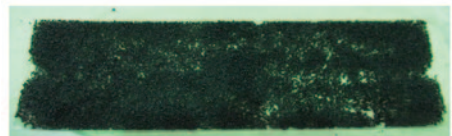


Surface of a granule

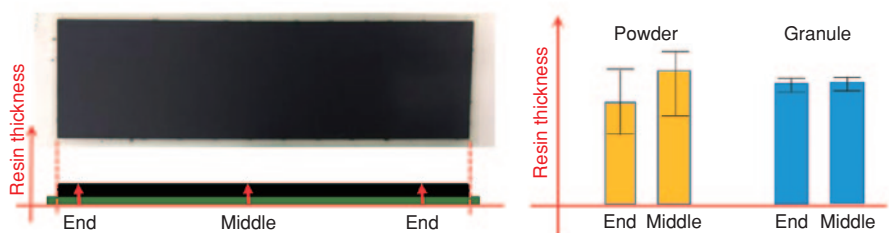
Figure 2 Granule particle distribution and the surface of a granule



Uniformity of a powder-type encapsulating compound

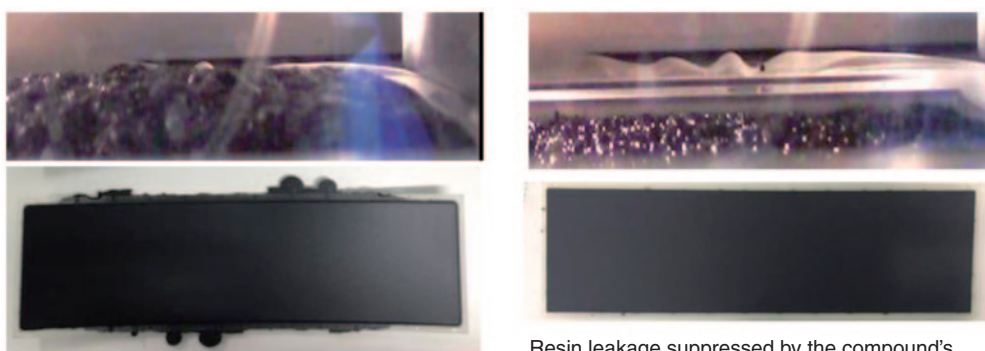


Uniformity of a granule-type encapsulating compound



Comparison of dimensional stability

Figure 3 Molding results



Resin leakage due to foaming

Resin leakage suppressed by the compound's de-foaming property

Figure 4 Evaluation of resin leakage when using the new compound

## 5 Future Business Development

- Sales promotion of developed material
- Further miniaturization
- Application of developed technologies to produce encapsulating compounds with high thermal conductivity and mold underfill materials

# Photosensitive Insulation Film, “PV series”

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## 1 Abstract

In recent years, the growing need for more advanced, miniaturized package substrates calls for higher-density wiring. Vias for connecting the layers of these substrates are traditionally formed by using CO<sub>2</sub> laser ablation technology. Generally, this technology is only capable of producing vias of 40 μm in diameter or larger. This limitation on the via diameter is an obstacle to achieving finer wiring. To address the demand for finer wiring, we have developed a photosensitive insulation film, called the PV series.

The PV series is capable of forming vias as small as 15 μm in diameter, and can form multiple interlayer vias through a photolithography process involving one-shot exposure. Furthermore, the PV series can be applied to the manufacturing of package substrates without requiring any additional processes. As such, the PV series makes it possible to manufacture highly advanced, miniaturized package substrates that offer high throughput and superior reliability.

## 2 Characteristics of the Product

- Capable of forming interlayer connecting vias 40 μm or less in diameter at once.
- Contributing to densification of package substrates without introducing special processes.
- Having excellent insulation reliability and reflow heat resistance and expressing high reliability.

## 3 Background of the Development

The number of interlayer connecting vias in the work area hereafter tends to increase due to the wiring densification of package substrates. The interlayer insulation film material to be used forms interlayer connecting vias by irradiating with a CO<sub>2</sub> laser. Since it is generally difficult to form vias of 40 μm or less in diameter by the laser, a problem arises against densification of wiring as the increase in the number of vias accompanies the increase in the processing time. Then we developed a photosensitive interlayer insulation film called the PV series by combining our proprietary photosensitive resin technology and insulation resin technology. The advantage of the developed PV series is shown in **Figure 1**. Upon the development of the PV series, we fused our proprietary photosensitive resin technology and insulation resin technology in response to the densification by implementing the general package substrate manufacturing processes.

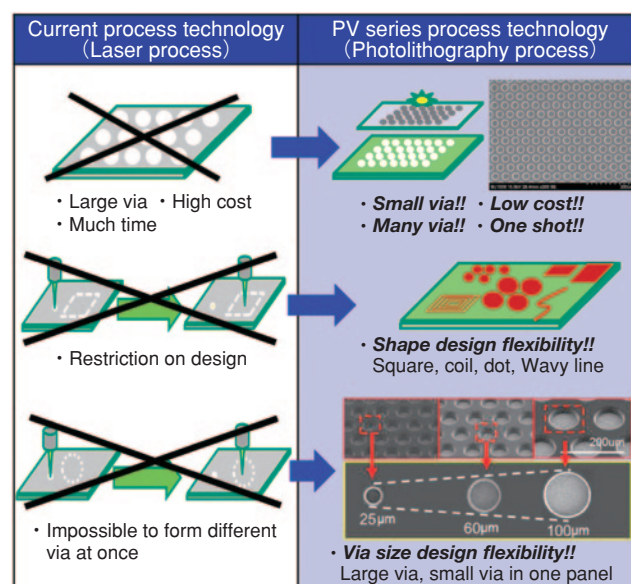


Figure 1 Advantage of PV series



## 4 Technical Details

### (1) Via opening characteristics of PV-F008

The developed PV-F008 can form vias with a small diameter of 15  $\mu\text{m}$ , which are difficult to form by  $\text{CO}_2$  laser. In addition, non-circular vias represented by square vias can be processed at once (**Figure 2**), and the via processing time can be reduced significantly.

### (2) General characteristics of PV-F008

The PV-F008 is suitable for the semi-additive construction method in addition to the photolithography. **Table 1** shows the general properties of the PV-F008. The via shape of the PV-F008 is represented by top/bottom sizes of 50  $\mu\text{m}$ /40  $\mu\text{m}$ , and PV-F008 has excellent via forming ability. In addition, the high adhesion (0.6 kN/m) of PV-F008 with electroless plated copper enables the suppression of the peeling of the wiring at the time of fine wiring patterning. Furthermore, reflow heat resistance of a multi-layer substrate assumed to be a package substrate and high insulation durability in a line and space of 12  $\mu\text{m}$  and 12  $\mu\text{m}$ , respectively, and an interlayer space of 15  $\mu\text{m}$  are excellent.

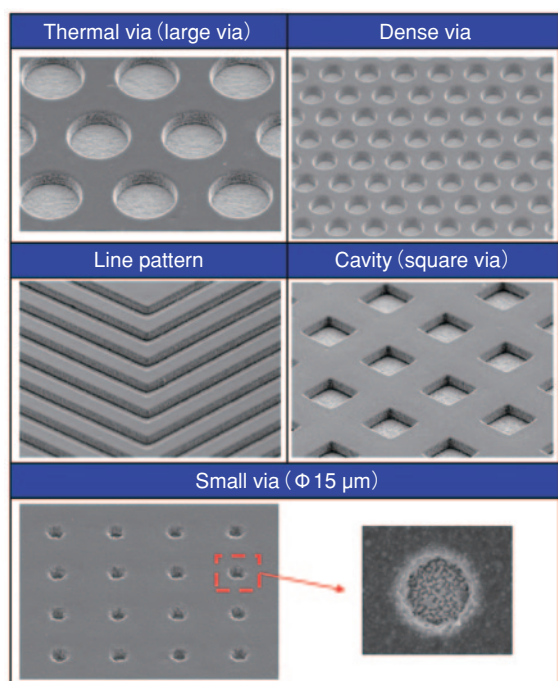


Figure 2 Photolithography of PV-F008

Table 1 Properties of PV-F008

Item		Unit	PV-F008
Minimum via	Resin thickness 10 $\mu\text{m}$	$\mu\text{m } \Phi$	15
Via size (Top / Bottom)	$\Phi$ 50 $\mu\text{m}$ target	$\mu\text{m } \Phi$	50 / 40
Insulation reliability (HAST 130°C, 85% RH)	Layer to layer (15 $\mu\text{m}$ )	200 h	Pass
	Line / Space=12 / 12 $\mu\text{m}$	200 h	Pass
TCT resistance	-65°C $\leftrightarrow$ 150°C	1000 cycle	Pass
Reflow cycle resistance	260°C reflow	Cycle	20
Peel strength	Cu plating	kN/m	0.60

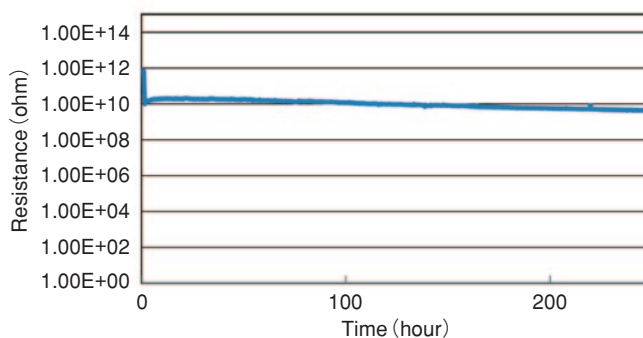


Figure 3 HAST resistance of PV-F008

## 5 Future Business Development

- Expansion of sales and application of developed product.
- Development of photosensitive insulation material for the next generation.

# Dry Film Resists for Fine Line and Space Patterning, “RY-5100UT series”

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## 1 Abstract

Photosensitive dry film resist has been used for circuit patterning in the printed wiring board (PWB) of various devices such as smartphones and central servers. To address the need for information processing at higher speeds and of larger volumes of data, we need to mount higher-performance PWBs in electronic devices by using finely patterned circuits.

The RY-5100UT-series photosensitive dry film for fine line and space patterning that we developed improves upon conventional photosensitive dry films.

RY-5100UT enables circuit patterning of 2  $\mu\text{m}$  resolution on full-size PWBs. We expect that demand for RY-5100UT will increase in the future, as the need for ever smaller, thinner, and higher-performance electronic devices grows.

## 2 Characteristics of the Product

- The developed product exhibits excellent adhesion to substrates, and offers superior resolution and resist patterning.
- Few resist tails are generated, helping to reduce the undercut of the plating line.
- The developed product is compatible with projection exposure machines that use light sources with wavelengths of 355 nm.

## 3 Background of the Development

Semiconductor package (PKG) substrates are a type of printed wiring board mounted on electronic devices, such as smartphones and central servers. PKG substrates play an important role as the intermediate layer that connects the IC chips that process information to the PWB side. To address the need for increased information-processing capacity in recent years, the wiring of IC chips is becoming more and more miniature. Relative to the miniaturization of IC chips, the miniaturization of wiring for PWBs and PKG substrates has been slow, and the loss of energy due to differences in circuit widths has reached a level that can no longer be ignored.<sup>1)</sup> To address this problem, PWB manufacturers have developed new PKG substrates with different structures. However, because it was necessary to significantly reduce the width of conventional circuits, the use of a liquid resist (which had proven results when used in wafer-level packages) as the resist for circuit patterning has become mainstream.<sup>2)</sup> Still, it is difficult to evenly apply a liquid resist to large panels. Furthermore, developing solutions and stripping solutions have never actually been used by conventional PWB manufacturers, and liquid resists require the use of expensive organic materials. For these reasons, there is strong demand for a photosensitive dry film that allows, as much as possible, the continued use of existing equipment and chemicals.

In light of this situation, we began developing a photosensitive dry film that enables the patterning of fine circuits.

## 4 Technical Details

Semiconductor package substrates are usually manufactured by using the semi-additive process (SAP) method.<sup>3)</sup> **Figure 1** shows a diagram indicating the circuit width. Although the circuit pitch of a conventional semiconductor PKG substrate is 20  $\mu\text{m}$ , the new package structure that uses fine circuit patterning requires circuit patterning with a pitch of between 4  $\mu\text{m}$  and 10  $\mu\text{m}$ . To respond to such rapid miniaturization, we developed the RY-5100UT series, which adopts a new hydrophobic material that effectively suppresses expansion caused by sodium-carbonate developing solutions. We also identified a photosensitizer suitable for high-resolution projection exposure machines and the optimum exposure region. The properties of the RY-5100UT series are listed in **Table 1**.

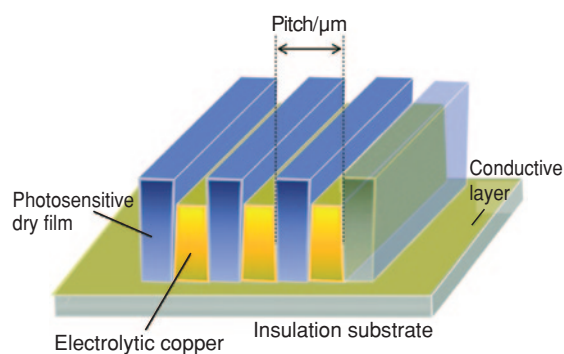


Figure 1 Pitch of the circuit width

Table 1 Properties of the RY-5100UT series

Item	Unit	RY-5110UT	RY-5107UT
Exposure machine	—	Projection exposure machine	
Resist film thickness	μm	10	7
Developing time	s	10	7
Amount of exposure	mJ/cm <sup>2</sup>	200	200
Minimum circuit pitch	μm	6	4

Note: Recommended exposure machine, twice the minimum developing time, projection exposure machine: UX-44101SM-XJ01 (Ushio, Inc.)

Usually, when a fine circuit is patterned by using the SAP method, a projection exposure machine is used. Because a direct exposure machine or collimated light exposure machine is often used for conventional photosensitive films<sup>3)</sup>, these exposure machines must be matched to the projection exposure machine. By designing a resin that controls the photo-curing reaction, we were able to improve the reactivity and adhesion between the resist and the substrate interface. **Figure 2** shows a model of the photo-curing reaction.

By improving the reactivity and adhesion, the deformation of resist during plating deposition was reduced. Thus, we achieved a minimum circuit pitch of 4 μm after flash etching. **Figure 3** shows the results after plating and flash etching.

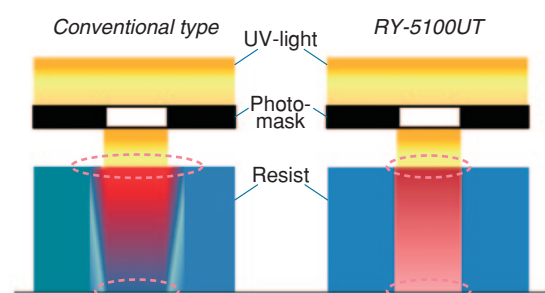
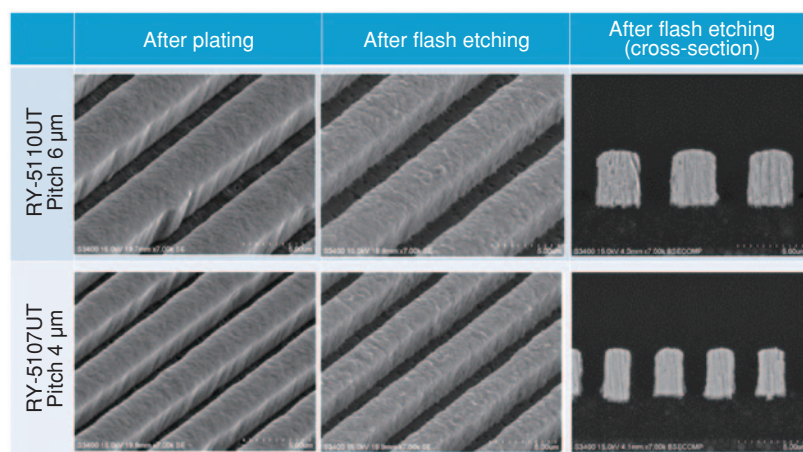


Figure 2 Photoreaction models for dry films for fine line patterning and space patterning



flash-etching solution : SAC (JCU CORPORATION)

Figure 3 SEM image of copper pattern after plating and flash etching

These results indicated that the RY-5100UT series offers both high resolution and high adhesion on a substrate and can be used to create fine resist patterns. As a material that can accommodate further miniaturization (which is expected to continue in the future), we believe that this new product will be useful in miniaturizing electronic devices and in improving the performance of such devices.

## 5 Future Business Development

- Further improvement of miniaturization ability of the photosensitive dry film.
- Expansion of the range of applications of the photosensitive dry film for fine circuit patterning.

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- 2) Noriyoshi Shimizu, Wataru Kaneda:Development of organic multi chip package for high performance application, 46<sup>th</sup> international Symposium on Microelectronics 2013.
- 3) Taiji Murakami, “Properties and Applications of Photosensitive Film,” Network Polymer, Vol. 34, No. 5, pp. 253–259 (2013)



# Halogen-Free Multilayer Material with Ultra-Low CTE and Low Elastic Modulus, “GEA-775G”

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## 1 Abstract

Semiconductor packages for smartphones and other electronic devices are becoming smaller, thinner, and higher in density. Recently, coreless substrates have attracted significant attention as a way to achieve thinner substrates, but coreless substrates present their own challenge, in that (compared to conventional substrates) they are more susceptible to warpage during the substrate process and during the packaging and assembly processes. To address this issue, Hitachi Chemical has developed the next generation in multilayer materials: GEA-775G, which is halogen-free and has an ultra-low CTE and a low elastic modulus. A comparison of the warpage during assembly when using the coreless substrate GEA-775G, to the warpage when using a conventional packaging material, indicated that the warpage of GEA-775G was 25% less than that of the conventional packaging material.

## 2 Characteristics of the Product

- Coreless construction method providing high resistance to warpage.
- Low thermal-expansion coefficient (5.0 ppm/°C).
- Low elastic modulus and high glass transition temperature (Tg).

## 3 Background of the Development

As the functionality of mobile devices, such as smartphones, becomes more sophisticated at an accelerated rate, the number of mounted components and the capacity of batteries must also be increased. Therefore, the miniaturization and slimming down of the main board on which the application processor is mounted are absolutely essential to effectively utilize a limited amount of space. This need drew our attention to the idea of using a coreless structure for construction of the main board. This coreless structure eliminates the core layers that are conventionally used, and consists only of insulation layers made of glass cloth impregnated with resin (hereinafter, “prepreg”). Although this allows us to produce a significantly thinner structure in comparison with the conventional structure, warpage often occurs as a result of the thermal history created during the mounting of semiconductor chips (hereinafter, “chips”) because no core layers exist to support the prepreg.<sup>1)</sup>

To address this issue, we began developing prepreg that is resistant to warpage and that can be used in the coreless structure. We successfully developed a type of prepreg called GEA-775G, which is characterized by a low thermal-expansion coefficient and a low elastic modulus.

## 4 Technical Details

### 1. Development concept for GEA-775G

The phenomenon of warpage generated due to the thermal history that is created during chip mounting is known to be caused by the difference in the thermal-expansion coefficient between the chip and the substrate.<sup>1)</sup> Therefore, it is necessary to make the thermal-expansion coefficient of the substrate close to that of the chip (3–4 ppm/°C). Furthermore, because the coreless substrate is subjected multiple times to press lamination by using the prepreg, it is also important to reduce the stress caused by thermal contraction during press lamination. **Figure 1** shows the resin design concept of GEA-775G. For the resin, we adopted a two-component system consisting of resin that can be broadly divided into the following types: an aromatic ring resin that easily takes the plane stack structure (for the high-elasticity segment), and a polymer alloy resin (for the low-elasticity segment). The high-elasticity segment ensured a higher Tg, and the low-elasticity segment ensured a lower elastic modulus. This low-elasticity segment reduced the elastic modulus to within the range where the thermal properties of glass cloth can be easily derived, and enabled us to achieve a reduction in the thermal-expansion coefficient.

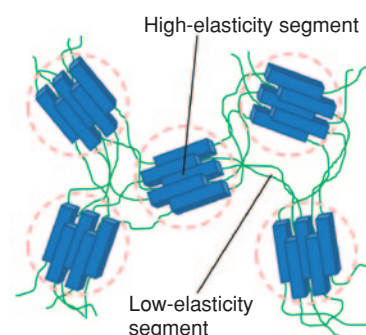


Figure 1 Resin design model of GEA-775G

### 2. General characteristics of GEA-775G

The general characteristics of the newly developed GEA-775G are shown in **Table 1**. For comparison, this table also includes the properties of another material previously developed by our company. The thermal-expansion coefficient ( $\alpha$  1) of GEA-775G

is 5.0 ppm/°C, which is approximately 17% lower than that of the other material. In addition, the new material's elastic moduli of 14 GPa at 30°C and 9 GPa at 260°C are significantly lower than the values for the previous material.

### 3. Warpage characteristics of GEA-775G

We evaluated the warpage properties of four-layer substrates using GEA-775G and four-layer substrates using our conventional material. The appearance and specifications of the evaluated packages, and the result of warpage at each temperature are shown in **Figures 2 and 3**, respectively. Colors are used to indicate degree of warpage measured at different temperatures: blue indicates warpage measured at 25°C before heating, red indicates warpage measured at 260°C, and green indicates warpage measured at 25°C after cooling. **Figure 3** shows that the change in the degree of warpage ( $\Delta$ ) for the package that used our conventional material was 360  $\mu\text{m}$ , while the change in the degree of warpage ( $\Delta$ ) in the package that used GEA-775G was 265  $\mu\text{m}$ . Using GEA-775G resulted in a reduction in warpage of approximately 25%.

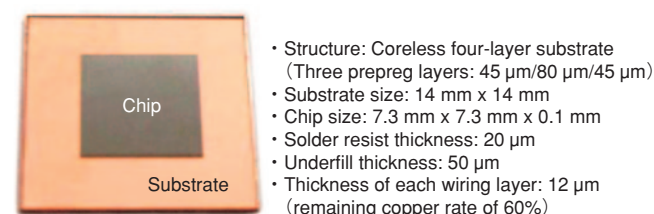


Figure 2 Structure of the package evaluated for warpage

Item	Condition	Unit	GEA-775G	Our conventional material
Prepreg thickness	—	$\mu\text{m}$	25	25
Glass cloth	—	—	S-glass	S-glass
Tg	DMA	°C	270	280
Thermal expansion coefficient <sup>1)</sup>	$\alpha 1$ (X,Y)	ppm/°C	5.0	6.0
	$\alpha 2$ (X,Y)		1.0	1.5
Storage modulus	30°C	GPa	14	18
	260°C		9	13
Copper foil peel strength	VLP-12 $\mu\text{m}$	kN/m	0.6	0.5
Dielectric constant <sup>2)</sup>	1 GHz	—	3.7	3.9
Dielectric dissipation factor <sup>2)</sup>	1 GHz	—	0.008	0.007

1) TMA (tensile) 2) SPDR method

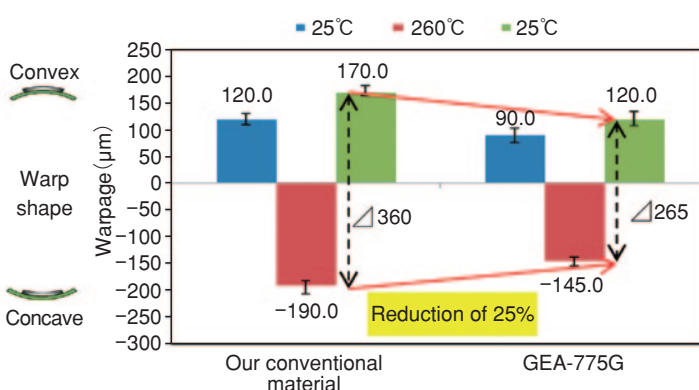


Figure 3 Results of the warpage evaluation

### 4. Evaluation of insulation performance

We evaluated conductive anodic filaments (CAF) between through holes (hereinafter, "TH"). **Figure 4** shows the structure of the substrate that was evaluated, as well as the test conditions, and **Figure 5** shows the results of the evaluation of CAF. Resistance values at distances between TH walls of 0.15 mm and 0.20 mm showed no reduction between the initial measurement and the measurement after 500 hours had passed, which indicates that the insulation performance of GEA-775G is good.

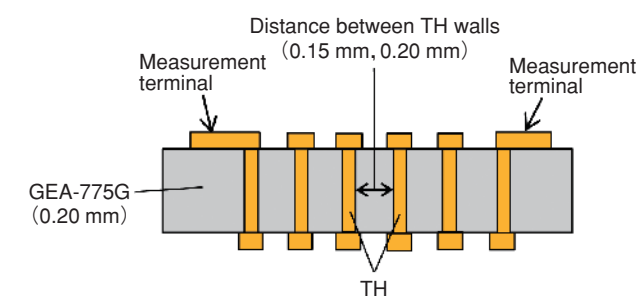


Figure 4 Structure of the substrate evaluated for insulation performance

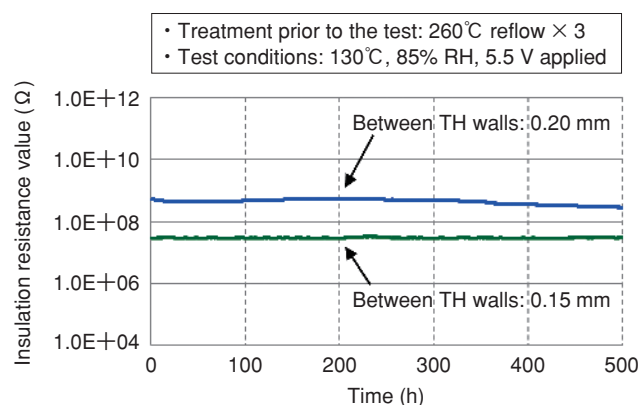


Figure 5 Results of the insulation evaluation

## 5 Future Business Development

- Development of a multilayer material with low thermal expansion and low elasticity with the goal of further reducing package warpage

### [Reference]

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# Copper-Clad Stretchable and Flexible Film

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## 1 Abstract

In recent years, wearable devices that track vital signs and that can be worn under, with, or on top of clothes or skin, have been attracting a lot of attention. Among wearable devices, the market for stretchable devices in particular is expected to grow. In light of such circumstances, we have developed a new material to be used to manufacture such devices. This new material consists of elastic film that is laminated with copper foil and is resistant to high temperatures. The elastic film has excellent mechanical properties: it is capable of elongating by 550% and has a recovery rate of 94%. In addition, this material is resistant to both the chemicals and the heat associated with the subtractive process and the N<sub>2</sub> reflow process. Furthermore, the material has a low dielectric constant (Dk) of 2.3 at 10 GHz, and a dielectric dissipation factor (Df) of 0.0030 at 10 GHz. Both of these properties are important for flexible substrates used in high-frequency devices.

## 2 Characteristics of the Product

- The film offers stable conductivity, with little change in the film's wiring resistance even when it is stretched.
- The film's low dielectric constant and low dielectric dissipation factor mean that energy conservation can be expected in high-frequency regions.
- The film is compatible with existing processes for forming and mounting circuits, so you do not need to invest in new facilities or equipment.

## 3 Background of the Development

Recently, the Internet of Things (which is commonly referred to as "IoT" and describes a state in which various things are connected via the internet) has attracted a lot of attention, and wearable devices<sup>1), 2)</sup> are being developed as a new type of device. In light of these trends, wearable devices not only need to provide the same functions as conventional devices, but also need to be comfortable. This requirement has led to studies on the application of stretchable devices to curved surfaces (such as a human body).<sup>3)</sup> As the conductor for such stretchable devices, the use of a stretchable, conductive paste has been examined. However, because such pastes typically contain a metal filler to ensure conductivity, repeated straining of the paste leads to an increase in its resistance value, which poses an issue.<sup>4)</sup> Although a flexible print circuit board can be used to stabilize the resistance value, it is difficult to miniaturize such circuit boards or to make them conform to a particular shape. For these reasons, we attempted to develop a new wiring material for stretchable devices that maintains a stable resistance value even when subject to repeated bending or straining, and that can be made to conform to a particular shape.

## 4 Technical Details

### 1. Design concept of the stretchable wiring material

In order to be used as a conductor in stretchable devices, the base material must be highly malleable, must maintain a stable resistance value when stretched, and must be sufficiently heat-resistant to enable the mounting of parts. To satisfy these requirements, we developed a stretchable wiring material by integrating technologies used in print circuit boards and composite materials. To make the conductor stretchable, we used multiple layers consisting of a layer of etched copper foil in a meander structure, and a base layer of a stretchable and highly heat-resistant film made from a combination of elastomer and thermosetting resin.

### 2. General properties of the stretchable wiring material

Table 1 shows the general properties of the stretchable wiring material. The base material can elongate by 550% before breaking, and has a 94% recovery rate after being elongated by 50%. Furthermore, the material's resistance to the chemicals used during wiring forming and its superior heat resistance make it suitable for use in conventional etching and soldering processes.

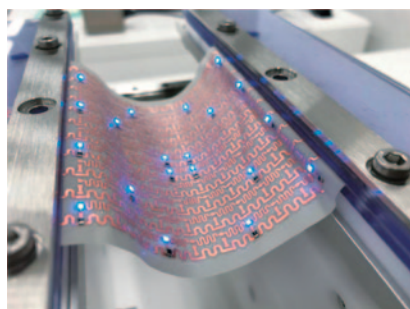


Figure 1 A sample device (upper) and structure of copper-clad stretchable and flexible film (lower)

Table 1 Properties of the elastic film used for the copper-clad stretchable and flexible film

Item	Property	Note
Tensile elongation	550%	Film thickness: 100 μm
Tensile modulus	5.0 MPa	
Recovery rate	95%	
Peel strength (copper foil)	> 1.0 kN/m	90° peel
Dielectric constant (Dk)	2.3	At 10 GHz, using the cavity perturbation method
Dielectric dissipation factor (Df)	0.0030	At 10 GHz, using the cavity perturbation method
Breakdown voltage	7.0 kV	Film thickness: 80 μm
Heat resistance	No change	260°C, 10 s, 10 cycles in an N <sub>2</sub> atmosphere
Chemical resistance	NaOH	No change
	Na <sub>2</sub> CO <sub>3</sub>	No change
	Copper etchant	No change

**Figure 2** shows the correlation between the change observed in the wiring resistance of the base material (after forming), and its rate of elongation. These results indicate that, even when the base material is elongated by 90%, the resistance changes by no more than 5%. Similarly, **Figure 3** shows the change observed in the wiring resistance when the base material was repeatedly stretched by 10%. These results indicate that, even after being stretched 15,000 times, the stretchable wiring material shows little change in wiring resistance. Furthermore, the material has a low dielectric constant (Dk) of 2.3 at 10 GHz and a low dielectric dissipation factor (Df) of 0.0030 at 10 GHz.

Based on these results, we believe this new stretchable wiring material can be applied to various types of stretchable devices.

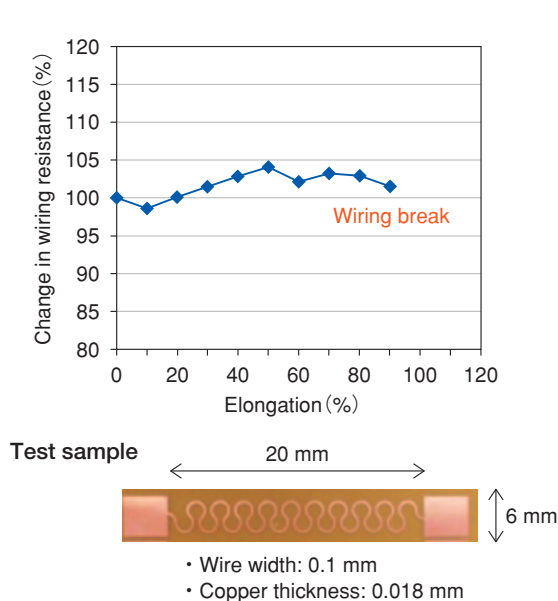


Figure 2 Change in wiring resistance when stretched

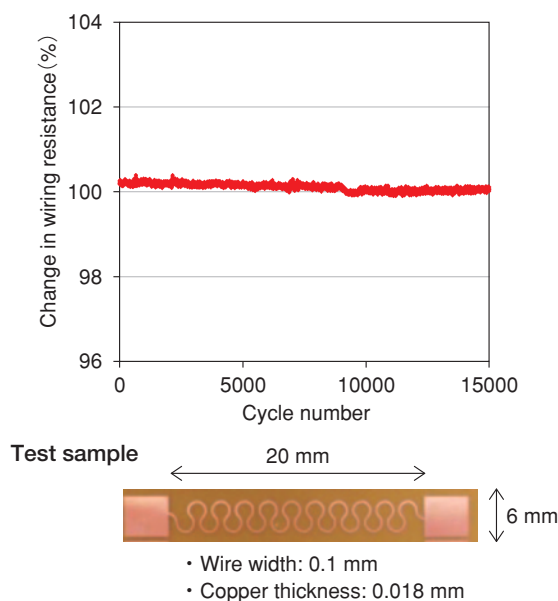


Figure 3 Change in wiring resistance during stretching test cycles under a 10% tensile strain

## 5 Future Business Development

- Development of low thermal expansion materials.
- Development of highly adhesive, stretchable materials for wire insulation.
- Development of semi-stretchable, highly flexible wiring materials for high-frequency (5G) applications.

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# Sintered, Highly Wear-Resistant Material for Turbochargers

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## 1 Abstract

From the viewpoint of improving fuel economy and regulating the exhaust gas of internal combustion engines, the boarding rate of turbochargers in passenger cars is increasing, in particular, for gasoline vehicles, where the boarding rate exceeds that of diesel vehicles.<sup>1)~4)</sup> In gasoline engines, because the temperature of exhaust gas released by turbochargers becomes quite high, austenitic high-chromium cast steel (hereinafter “high-chromium cast steel”), which has high wear-resistance and oxidation-resistance, is generally used for the heat-resistant bearings that control the flow rate of exhaust gas. However, as a result of the application of technologies to improve fuel economy (such as lean-burn engines), the temperature of exhaust gas now rises to near 1,273 K, precipitating the need for further wear resistance. To address this need, we developed a highly wear-resistant sintered alloy that consists of fine carbide dispersed in an austenitic stainless steel matrix, and takes advantage of the flexibility of the alloy designs characteristic of sintered materials.

## 2 Characteristics of the Product

- The material offers better wear-resistance and lower friction compared to high-chromium cast steel.
- The material offers the same level of resistance to oxidation as high-chromium cast steel.

## 3 Background of the Development

Sliding heat-resistant bearings are used in turbochargers to adjust the flow rate of exhaust gas. As such, these bearings must be highly resistant to both wear and oxidation. Conventionally, high-chromium cast steel has been used for these bearings. However, a problem where the rising temperature of exhaust gas led to bearings wearing down or becoming stuck, has prompted demand for even greater wear-resistance. In response to this demand and with the goal of breaking into the growing market for gasoline turbochargers, we began developing a sintered, highly wear-resistant material that offers better performance than high-chromium cast steel.

## 4 Technical Details

The material we developed uses an austenitic stainless steel matrix (Fe-Cr-Ni-Mo alloy), in which granular carbide is finely dispersed. **Figure 1** shows the microstructure of the material. The carbide-to-surface-area ratio of this material is about twice that of high-chromium cast steel. By using liquid phase sintering, we were able to achieve a high density of 7.3 Mg/m<sup>3</sup> and create a material that has isolated, fine pores. **Figures 2 and 3** show comparisons of the wear resistance and of the friction coefficient, respectively, between the new material and high-chromium cast steel. At 1,273 K, the amount of wear observed in the new material was approximately 30% of the amount of wear observed in the high-chromium cast steel, and the friction coefficient of the new material was lower and more stable than that of the high-chromium cast steel. These results can be attributed to the large number of fine carbide particles dispersed throughout the new material that help prevent adhesive wear. Similarly, **Figure 4** shows a comparison of the oxidation resistance between the two materials. The increase in the mass of the developed material due to oxidation is equivalent to that observed in the high-chromium cast steel, indicating that the new material has excellent oxidation-resistance. Main oxidation pathways lie in the chromium-depleted zones that form around pores and carbides, and the isolated, fine pores of the new material and the discontinuity of the chromium-depleted zone due to the pulverization of the carbide particles are believed to slow the progress of oxidation.<sup>5)</sup>

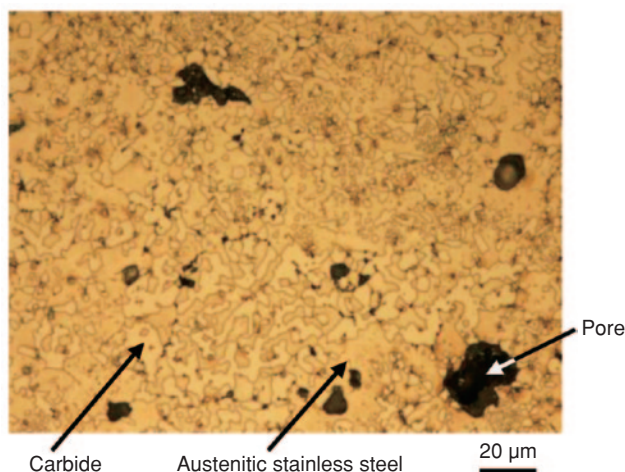


Figure 1 Microstructure of the developed material

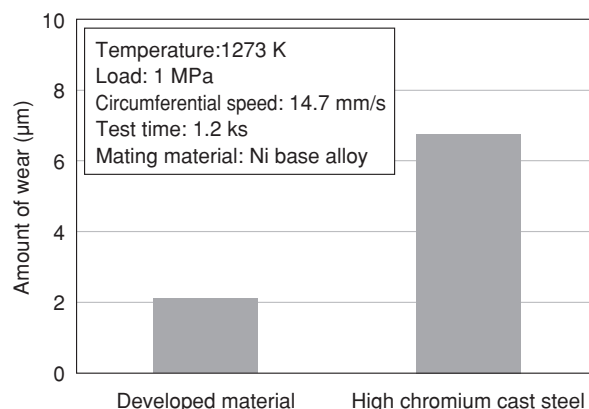


Figure 2 Results of the wear test

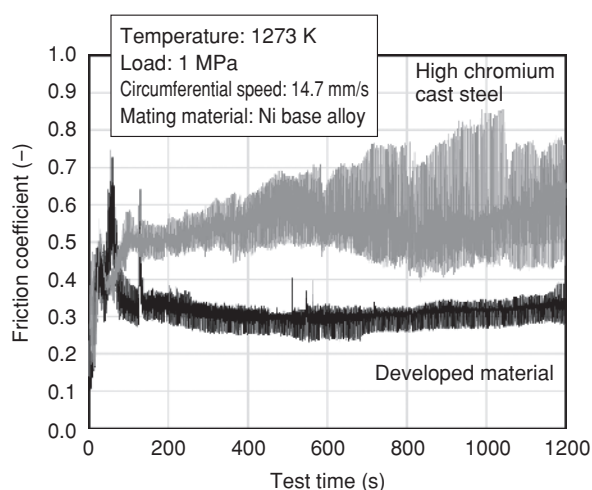


Figure 3 Friction coefficient during the wear test

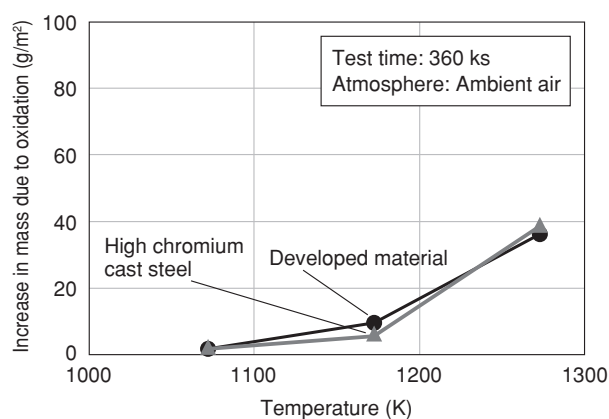


Figure 4 Increase in mass after the oxidation test

## 5 Future Business Development

Achieving high wear-resistance and high strength at high temperatures

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### [Relevant patents]

Patent No. 5987284  
 Patent No. 5939384  
 Patent No. 6229277

# Resin-Encased, Metallized, Humidity-Resistant Film Capacitor, “MKCP4T”

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## 1 Abstract

In recent years, an increasing number of renewable energy systems now use film capacitors, which last longer than aluminum electrolytic capacitors, for their DC link circuits. Today, there is a growing need for film capacitors that meet the UL-94 flammability standard's V-0 rating, and that are long-lasting and humidity-resistant.

Achieving both flame retardancy and humidity resistance is difficult, because a side effect of adding flame retardants to resin is a decrease in humidity resistance. Lower humidity resistance allows moisture to enter the capacitor, which in turn can shorten the capacitor's lifespan. As such, there is a need to improve the case and filler resin of encased film capacitors.<sup>1)</sup>

To this end, we developed the new MKCP4T series of capacitors that use thinner dielectric film, as well as a new outer case and epoxy resin. These adaptations allow MKCP4T capacitors to achieve both flame retardancy and humidity resistance, with specifications of 1,000 hours at 85°C and 85% RH, guaranteed.

## 2 Characteristics of the Product

- Resin-encased film capacitor that offers both humidity resistance and flame retardancy, and that is suitable for DC link circuits used in high-humidity environments.
- Guaranteed specifications of 1000 hours at 85°C and 85% RH.
- Outer case and filler resin that meet the UL-94 V-0 rating for flame retardancy.

## 3 Background of the Development

Usually, DC link circuits use aluminum electrolytic capacitors that have a large electrostatic capacity per unit volume. Disadvantages of aluminum electrolytic capacitors include a large dielectric loss tangent ( $\tan \delta$ ) and a short actual service life of 5 to 10 years. In contrast, while film capacitors have a smaller electrostatic capacity relative to aluminum electrolytic capacitors, film capacitors offer the advantages of a small  $\tan \delta$  and a longer actual service life of 10 to 15 years. For these reasons, recent years have seen an increase in the use of film capacitors in DC link circuits. In particular, the use of such capacitors has increased in the field of renewable energy, as a way to conserve the time and money spent maintaining devices. As such, there is demand to further extend the actual service life of film capacitors to 20 to 25 years.

There is also strong demand for flame-retardant film capacitors. However, it is difficult to simultaneously improve flame retardancy and extend the service life, as these properties have a trade-off relationship. In this paper, we examine how to make resin-encased film capacitors flame-retardant while also extending their service life. To evaluate these properties, we performed a high-temperature and high-humidity bias test (THB test) at 85°C and 85% RH. This test is an accelerated test that allows us to estimate the actual service life. A result of 1,000 hours under these test conditions corresponds to an actual service life of 20 years.<sup>2)</sup>

## 4 Technical Details

The MKCP4T series we developed uses parts with improved humidity resistance, which helps prevent moisture from entering the capacitor and in turn guarantees specifications of 1,000 hours at 85°C and 85% RH. **Table 1** lists the capacitor's specifications. A polyphenylene-sulfide (PPS) material that helps prevent the infiltration of moisture is used for the outer case. (See **Figure 1**.) As a new sealing resin, we used an epoxy resin, which offers both humidity resistance and flame retardancy. In addition, by using a thinner dielectric film, we were able to miniaturize the condenser parts and increase the amount of filler resin, helping to prevent moisture from entering the device.

By applying the newly developed MKCP4T series, we achieved a capacity change rate of under  $\pm 5\%$  after 1,000 hours of THB testing. (See **Figure 2**.)

Table 1 Specifications

Item	Description		
Operating temperature	-40 ~ +105°C		
Rated voltage UN	700 Vdc	900 Vdc	1100 Vdc
Capacitance	15 ~ 80 $\mu\text{F}$	9 ~ 40 $\mu\text{F}$	6 ~ 30 $\mu\text{F}$
Dimensions [T×H×L]	21.5 mm × 38.5 mm × 43.0 mm ~ 35.0 mm × 60.0 mm × 57.5 mm		
Capacitance tolerance	$\pm 10\%$		
Dielectric	Polypropylene		
Humidity resistance	85°C 85% RH with UN, 1000 h, $\Delta C \leq \pm 5\%$		
Standards	IEC61071 : 2007		
Electrode	No internal safety device		
Case and filling material	UL94V-0		
Environmental regulation	Comply with RoHS		

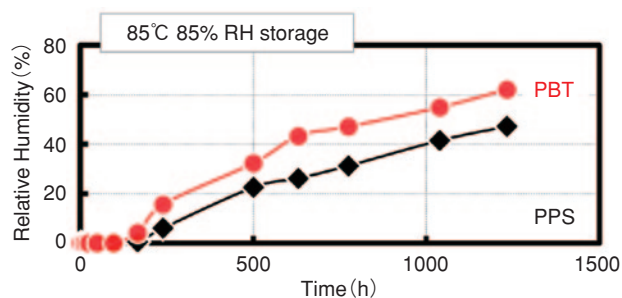


Figure 1 Moisture infiltration results

\* preparation  
Embed temperature sensor to PPS and PBT cases and sealed with epoxy resin  
\* Testing  
Place samples in high temperature / humidity oven (85°C 85%)  
Calculated water penetration amount by sensor value

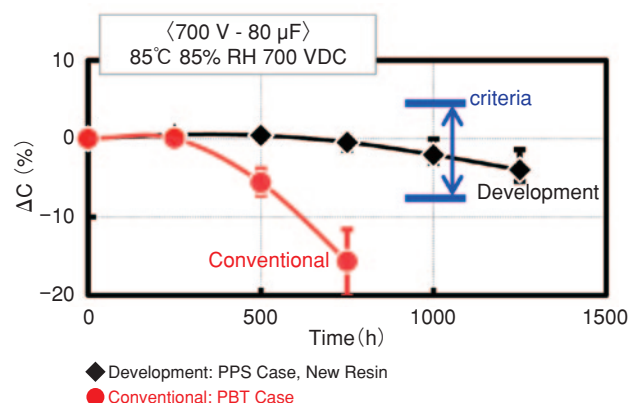


Figure 2 THB test results

## 5 Future Business Development

- Additional of products with a rated voltage of 450 V.
- Addition of large products of at least 45 mm in thickness and 80 mm in height.
- Development of products with guaranteed specifications of 1,500 hours at 85°C and 85% RH.

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# Non-fluid Latent Thermal Storage Material

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## 1 Abstract

Methods for handling heat vary greatly depending on the environment. For example, heat can be handled as energy or as something to be disposed of. In the former case, there is demand for technologies for utilizing waste heat from the perspective of saving energy. In the latter case, there is demand for technologies for releasing heat and for cooling in order to suppress rises in the temperatures of electronic devices associated with the high-density integration of increasingly smaller semiconductor packages. To address both of these issues, we focused on developing a latent thermal storage material that can retain and absorb heat. The latent thermal storage material we developed is a type of phase change material (PCM). The thermal storage performance of PCMs is most effective at the temperature where the material changes phases from a solid to a liquid. To expand the applicability of PCMs, we have developed a PCM that does not flow even as it changes phases, and have evaluated its effectiveness.

## 2 Characteristics of the Developed Product

- The material does not flow above the phase change temperatures.
- The material exhibits excellent thermal storage performance, as well as strength and flexibility.
- The form of the material can be fixed after the filling and coating processes.

## 3 Background of the Development

The latent thermal storage material exhibits thermal storage properties at certain temperatures (the melting point and the boiling point) as it changes phases from a solid to a liquid or from a liquid to a gas. Therefore, the material has limited applications and can only be used inside sealed structures. As a way to suppress phase changes, the microencapsulation of the latent thermal storage component has been investigated.<sup>1)</sup> The material comprises a thermal storage component (associated with the solid-to-liquid phase change), such as an n-paraffin, encapsulated in a polymer component, such as melamine or acrylic resin. This polymer shell allows the material to maintain its shape even when it liquefies at temperatures exceeding the phase-change point. However, because the powder-like capsules have a diameter of only several tens to several hundreds of micrometers, the molded material cannot maintain its shape unless it is combined with a binder. In addition, a high level of filling inside the binder is required in order to improve the thermal storage performance, but it is difficult to achieve a mixture that has both sufficient strength and flexibility.

By applying our technologies related to the design of polymer molecules as well as our mixing and dispersing technologies used in composite materials, we have developed a non-fluid latent thermal storage material that has excellent thermal storage performance while also retaining its strength and flexibility.

## 4 Technical Details

### (1) Conceptual diagram of the material

**Figure 1** shows a conceptual diagram of the material.

As shown in (a), normal latent thermal storage materials melt and become fluid at temperatures exceeding the phase-change point. To prevent the material from becoming fluid, we developed materials via two different methods as shown in (b) and (c). In (b), we achieved non-fluidity by containing crystal components in a polymer matrix. In (c), the same was achieved by making the crystal structures bond with the side chains of a polymer. Furthermore, by introducing a functional group capable of a crosslinking reaction, the material in (c) can be filled into a complex shape or hardened after coating.

### (2) Characteristic of the material: Effective in suppressing rises in temperature

As shown in **Figure 2**, we verified the effectiveness of the developed material in suppressing rises in temperature, by using

a PV module, on the back sheet of which the thermal storage material was attached. **Figure 2** also gives an overview of the measurement.

**Figure 3** shows the measured results for (a) the temperature of the surface of the back sheet and (b) the power generation characteristic associated with changes in temperature after irradiation by a solar simulator. The power generation characteristic is given in terms of maximum power ( $P_{\max}$ ).

The results indicated that rises in temperature were suppressed near the melting point of the thermal storage material. In addition, although the power generation characteristic tended to decrease as the temperature rose, this decrease was mitigated by reducing the speed at which the temperature rose.

Table 1 Example of feature for non-fluidity thermal storage material and assumption product form

Item	Unit	Thermal storage material being developed		
Sample name	—	A	B	C
Composition	—	Composite		Polymer
Phase-change point (melting point)	°C	18	75	35
Heat of fusion	J/g	137	143	71
Assumed product form	—	Sheet		• Sheet • Paste (curable)

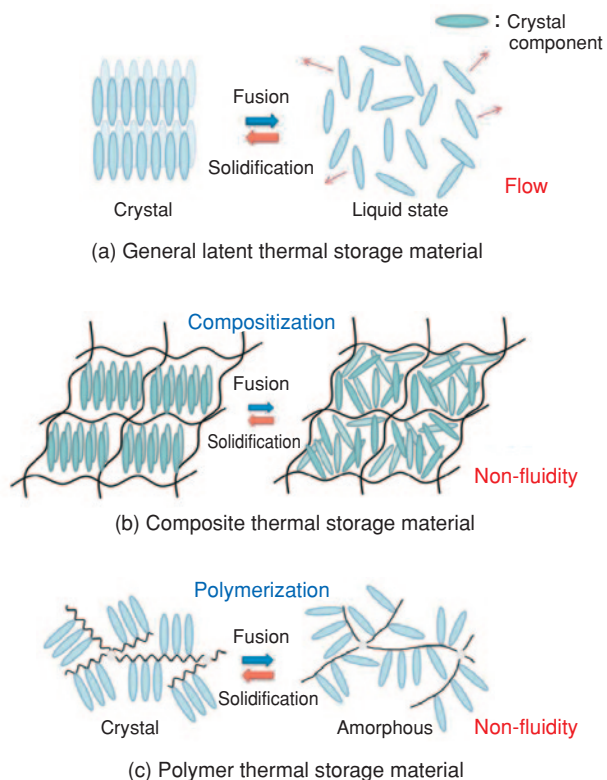


Figure 1 Conceptual diagram of phase change of latent thermal storage material

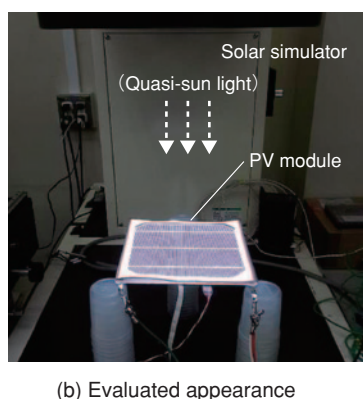
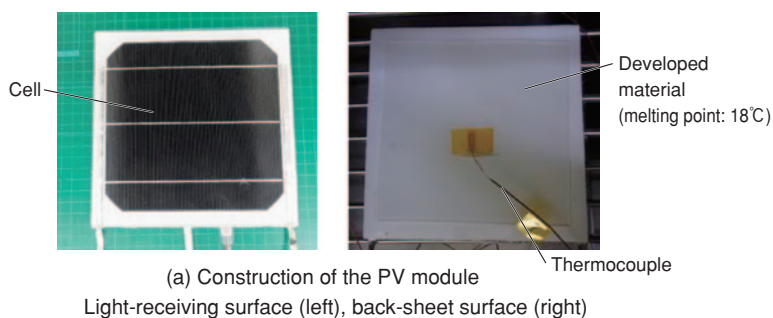


Figure 2 Evaluation overview of PV module

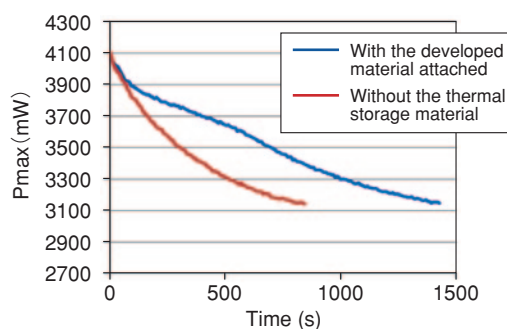
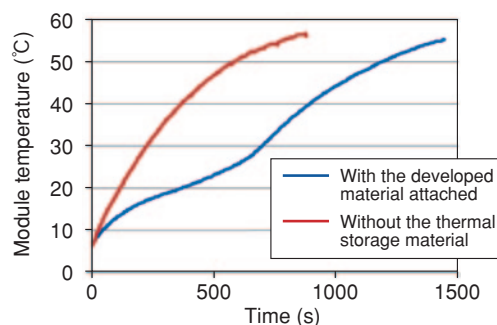


Figure 3 Effect of latent thermal storage material

## 5 Future Business Development

- New applications as a heat absorbing material.

### [Relevant patent]

- 1) Japanese Patent No. 5651272

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