Open Innovative Activity of Total Solution for Semiconductor Packaging

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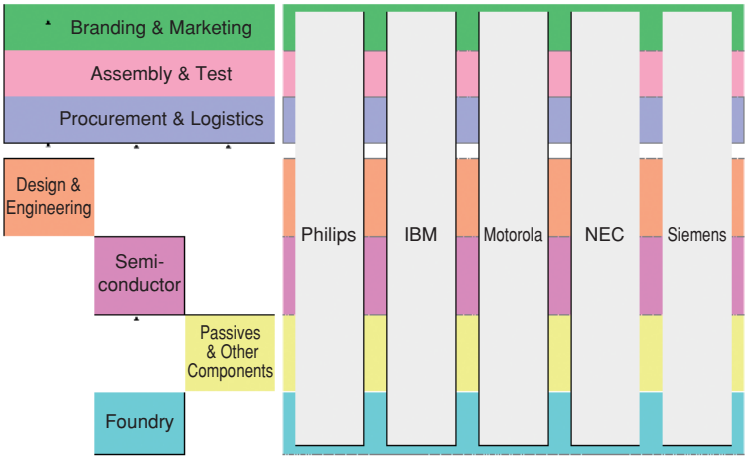
Since the 21st century began, the mainstream of the supply chain of the semiconductor package industry has changed from vertical integration to a horizontal specialization model. The twilight of Moore's law, which has been a driver of the electronics industry for the past half century, is becoming apparent and the barrier of 5 nm coming in several years is convincing. Recently, packaging technology is strongly expected to lead the continued progress of the system performance of electronic devices. In this situation, the strategy of the packaging material business of Hitachi Chemical is dynamically changing. This article describes open innovation through co-creation with other companies and organizations, based on Hitachi Chemical's open laboratory, founded with a state-of-the-art full assembly line in 2014 at the former Tsukuba Research Laboratory (currently the Core Technology Center). It also describes the creation and proposal of a total solution of a brand new semiconductor package, unifying material, equipment and process.

1 Introduction

The supply chains for semiconductors during the period from 1980 to 2000 are shown in **Figure 1**. As shown on the right side of the diagram, vertical integration models by large-scale semiconductor manufacturers (referred to as integrated device manufacturers or IDMs) were typical. However, in the 21st century, horizontal specialization based on functional differentiation began to spread (as indicated on the left of the diagram from "Branding & Marketing" to "Foundry"). IDMs, which had been responsible for both manufacturing semiconductor wafers and assembling semiconductor packaging, transformed into enterprises called foundries and companies that handle OSAT (outsourced assembly and test), respectively. Furthermore, as the latest movement, the largest foundry, Taiwan Semiconductor Manufacturing Co., Ltd. (TSMC), not only manufactures semiconductor wafers, but also handles a part of the package assembly process using the manufactured semiconductor wafers. Although these are the main industry types where companies use packaging materials in manufacturing, design houses (enterprises that design semiconductor packages, outsource the manufacturing, and then sell the finished products) and other enterprises that use this business model (designing and selling the finished products but outsourcing manufacturing) are gaining power. (An example of an enterprise that uses this business model is Apple Inc. in the United States.) As a result of this trend, to propose total solutions for semiconductor packages, we need to approach many different customers from various angles.



(Reference: Prismark Partners LLC, ELECTRONICS SUPPLY CHAIN REPORTER Q3 2016)

Figure 1 Supply chain of semiconductor products in 1980-2000

2 Status of Semiconductor Packaging Technology

The changes to technology nodes used in the mass production of semiconductor wafers are summarized in **Figure 2**. From this figure, it is obvious that refinement has been slowing down since 2009. The introduction of the 10 nm mass production process in 2017 and a plan for a 7 nm process have been announced. As such, the 5 nm process, which has long been considered the hurdle for CMOS, is expected to be achieved within the next several years. In the midst of these changes, three-dimensional technology has been rapidly developing for several years, and the actual application of such technology to memory has started.

With respect to NAND flash, the practical application of three-dimensional technology to memory cells has been achieved, allowing for further reduction of the bit unit price and high integration (two factors crucial to memory). On the other hand, with respect to DRAM, at present, three-dimensional technology relies on tip-to-tip or tip-to-wafer lamination using through-silicon electrodes (through-silicon via or TSV). (This type of lamination is referred to as 3D mounting.) As a result, higher integration, higher speed, and lower power consumption have been achieved, but the reduction in the bit unit price is still difficult.

Regarding logic semiconductors, a reduction in wafer yield due to the refinement of technology nodes (from 16 or 14 nm to 10 nm and then to 7 nm) has been predicted by various sources (**Figure 3**). As a countermeasure, a split-die package has been developed by using 2.5D mounting and silicon interposers.

As described previously, the refinement of technology nodes (which has continuously supported the evolution of the system performance of semiconductor products for more than a half century) is slowing down. In light of such circumstances, packaging technology is now expected to play a larger role in the advancement of semiconductor performance, to which end 3D mounting and 2.5D mounting using TSV have been developed. Furthermore, in the past two or three years, the fan-out package has attracted attention for the following reasons: the cost reduction in TSV processing has not progressed, the reduction in the thickness of the package for mobile devices is required in order to address heat radiation from heated chips, and the fan-out package has good high-frequency characteristics due to its short wiring length.

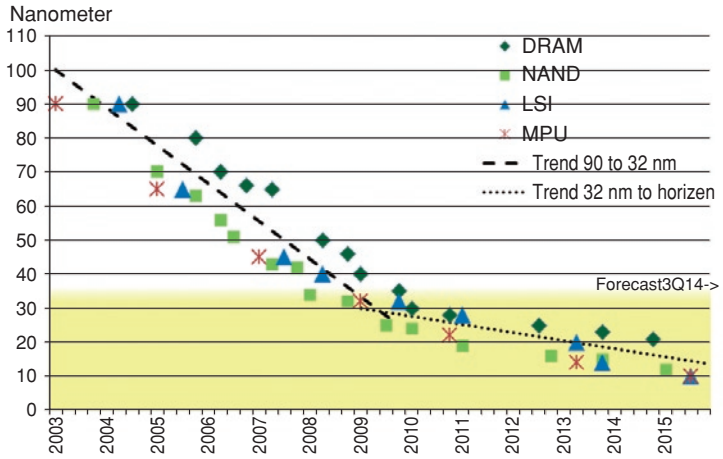
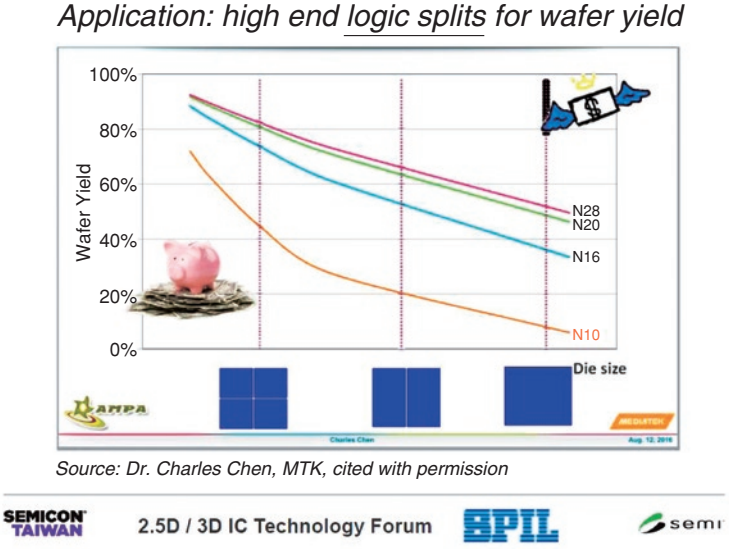


Figure 2 Volume production technology node transitions



(Reference: The handout distributed for Dr. Mike Ma's presentation at Semicon Taiwan 2016, SiP Global Summit 2016—2.5D/3D IC Packaging with Optical Technology Forum)
Figure 3 Relationship between technology node and wafer yield

3 Fan-Out Packages

"Fan-out package" is a generic term for a type of package where connecting terminals are arranged in a region larger than that of the chip. There are many types of fan-out packages. Although complicated configurations are sometimes required, for example, in the case of package-on-package (PoP) when connecting the top package to the bottom package, fan-out packages can be categorized into two main types: those created via the RDL-last method where redistribution lines (RDL) for fanning out are created on the semiconductor chip; and those created via the RDL-first method where a semiconductor chip is loaded onto the completed redistribution lines. Note that the RDL last method can be further categorized into face-up and face-down for a total of three fan-out package types (**Table 1**). In the RDL-last, face-up method, adhesives are applied to the back surface of a chip, which is then secured to the carrier material. Next, molding is performed and then the molding materials are ground to expose the chip terminal, thereby forming the redistribution layer. On the other hand, in the RDL-last, face-down method, adhesives are applied to the active surface of a chip, which is then secured to the carrier material. Next, molding is performed and then the carrier, adhesives, etc., are peeled back to expose the active surface on which the redistribution layer is formed. In the RDL-first method,

wiring layers are first formed such that the area in which each wiring layer is formed is larger than the size of the chip. Next, on the wiring layer, a semiconductor chip is loaded as a flip chip, and then the molding is sealed. The method used for wafers of 8 inches or 12 inches in size is generally referred to as the fan-out wafer level package (FO-WLP). Similarly, the method used for square wafers of 300 mm to 700 mm in size is generally referred to as the fan-out panel level package (FO-PLP). Various approaches to these methods have been proposed and applied depending on the specification of the package concerned, the required characteristics, and other conditions related to the infrastructure and technology of the manufacturer.

Table 1 Method classification of fan-out package

RDL-first	Face-down	×	Wafer level
RDL-last	Face-up		Panel level
	Face-down		

There are various methods for creating fan-out packages. The materials generally consist of carrier materials, temporary fixing materials, RDL insulating materials, wiring-forming photoresists, sealants, etc. Frequently used equipment include coating machines for liquid materials, laminators for film materials, back grinders for wafer processing, dicers, chip loaders, exposure and developing machines for processing photosensitive materials, compression molding machines, etc. Our company's product lineup includes many of these materials and equipment, many of which are installed in our open laboratory (**Figure 4**). In our packaging solution center, we work with various material-related departments and use the functions of the open laboratory to perform trial manufacturing of FO-WLP test vehicles (**Figure 5**). We are also working on proposing total solutions to customers and providing feedback to various material-related departments.

Figure 4 Hitachi Chemical Open Laboratory Concept and landscape photo

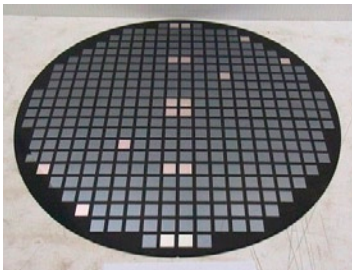


Figure 5 FO-WLP test vehicle made at Open Laboratory

4 Open Innovation and JOINT Project

Open laboratory was established and functions as a place for collaborative creation with semiconductor packaging-related customers, equipment and material manufacturers, etc. It is also a strategic tool for promoting open innovation. However, if we limit ourselves to using only our open laboratory facilities and our own products, it will be difficult for us to handle all cases (such as fan-out packages) that require novel, diverse, and speedy response. For this reason, in March 2016, we started the Jisso Open

Innovation Network of Tops project (JOINT), using equipment in cooperation with material manufacturers.

The trial manufacturing of test vehicles for fan-out packages of RDL-last, face-up type was carried out by outsourcing the processes of providing, forming, and delamination of temporary fixing materials to Tokyo Ohka Kogyo Co., Ltd.; the process of compression molding to Towa Co.; and the process of grinding molding materials to Disco Co. All other work was performed by our company. Similarly, the FO-PLP test vehicle trial manufacturing was carried out by using carrier glasses provided by Asahi Glass Co., Ltd., and by outsourcing the high-speed loading of a large amount of chips to Fuji Machine MFG. Co., Ltd. Although the project started in March, the quick action of each company made it possible to finish the trial manufacturing by the latter half of April. The actual test vehicles manufactured in both trials were introduced at ICEP 2016 (exhibition held in Sapporo in April 2016) and ECTC 2016 (exhibition held in Las Vegas, USA, in May 2016). These exhibitions are international conferences for packaging-related technology and attracted the attention of participants in the field (**Figure 6**). The JOINT project has achieved high-level trial manufacturing by assigning each process to a company with excellent skills in each field. Through this trial manufacturing, our final goal is to not only acquire know-how about each process from each company, but to also to work with all companies to propose a total solution for all of Japan. Such a solution would integrate conditions such as materials, equipment, and processes. Regarding semiconductor packaging processes that tend to be monopolized by equipment manufacturers or material manufacturers, it is sometimes difficult for individual companies to obtain general information about all processes of the trial manufacturing of the package. The trial manufacturing of the JOINT project is also expected to address such problems. In addition to the aforementioned companies, several other companies have expressed their intent to participate in the JOINT project. Thus, we hope to enlarge the collaborative network, propose a timely and adequate total solution for semiconductor packaging, and contribute to the expansion of the industry and of our company's business.

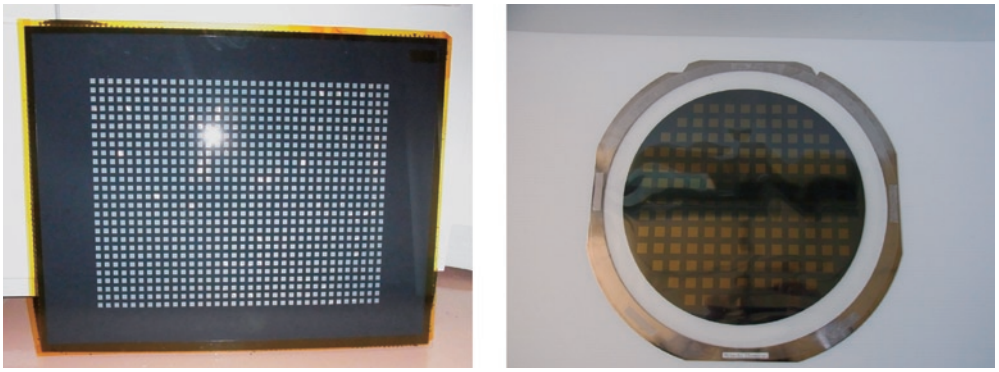


Figure 6 FO-PLP and FO-WLP demonstration samples assembled by JOINT project

5 Conclusion

As a result of the JOINT project, research and development is now performed in places outside of our company. In light of this, we plan to further expand the open laboratory (the key to proposing total solutions) in order to continue contributing to the semiconductor packaging industry, where supply chains and products continue to change. We hope to become the number one manufacturer of mounting materials in the world by implementing a cluster strategy for mounting materials. In FY 2016, we expanded the cleanroom inside a building at the current Tsukuba site and introduced new processing equipment. We are considering expanding or relocating to a place closer to the city in FY 2017 for the following purposes:

- To further promote open innovation
- To improve access from domestic and overseas customers and relevant companies such as JOINT project members
- To further cultivate open-mindedness

We are considering, if we do expand or relocate, to establish a consortium under the initiative of Hitachi Chemical as an advanced form of the JOINT project. In the semiconductor packaging industry, most parts of the supply chain are located overseas. We have already expanded our business overseas, with the current open laboratory acting as the global mother site to both the packaging solution center and open laboratory branches to be established in the future. We plan to enhance the functions of the packaging solution center as described above and, as a first step, we have started participating in the panel-level fan-out consortium held by Fraunhofer IZM in Germany. In the future, we hope to continue contributing to the mounting materials business, and to make our packaging solution center a global hub and an information-sharing base.