Technology Trends and Future History of Semiconductor Packaging Substrate Material

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The electronics industry has developed dramatically over the past half-century, primarily thanks to the semiconductor industry. Today, with increasing demand for smartphones and tablet computers, further high-volume, high speed, low power consumption LSIs and smaller/thinner semiconductor packages are strongly required. Meanwhile, the technical challenges involved in further fine pitch design shift the focus to assembly technology, which is considered the core technology required to achieve high-volume, high-integration semiconductor packages. Recently, the market for 3D semiconductor packages such as Package on Package (PoP), capable of stacking different IC packages such as memory and logic, is growing. Materials which have supported the development of such semiconductor packages include printed wiring board materials and semiconductor packaging materials. This report will introduce the history of printed wiring board materials and its technical trends in future.

1 Introduction

The electronics industry started with the commercialization of transistors in the 1950s, and has since grown into a ¥45 trillion market. Since personal computers (PCs) were introduced in the market in the late 1980s, the Internet and cell phones have become ubiquitous, and smartphones and tablet computers are recently growing markets. Electronic components and materials have supported the development of the electronics industry. Japanese semiconductors and electronic devices account for 20% of international markets, while the share of electronic components and materials exceeds 40%, reflecting the fact that the superiority of Japanese high-function materials is approved by the international community. The printed wiring board (PWB) is an electronic component incorporated in electronics, and comprising printed wiring board materials. Hitachi Chemical has developed advanced electronics technologies, and continuously marketed electronic materials that contribute to the electronic industry. This report presents the history, recent technical trends and future development of such printed wiring board materials.

2 What are Printed Wiring Board Materials?

The role of PWB is to transmit electric signals to electronic components such as semiconductor silicon chips incorporated into electronic equipment such as computers via copper circuits. **Figure 1** shows the hierarchical structure of silicon chips, semiconductor package substrates (“PKG substrates”), and PWB. The printed wiring board materials, including copper-clad laminate (core material), which is the base of PWB, photosensitive dry films for forming circuits and solder resist (**Figure 2**), compose the PKG substrate and PWB.

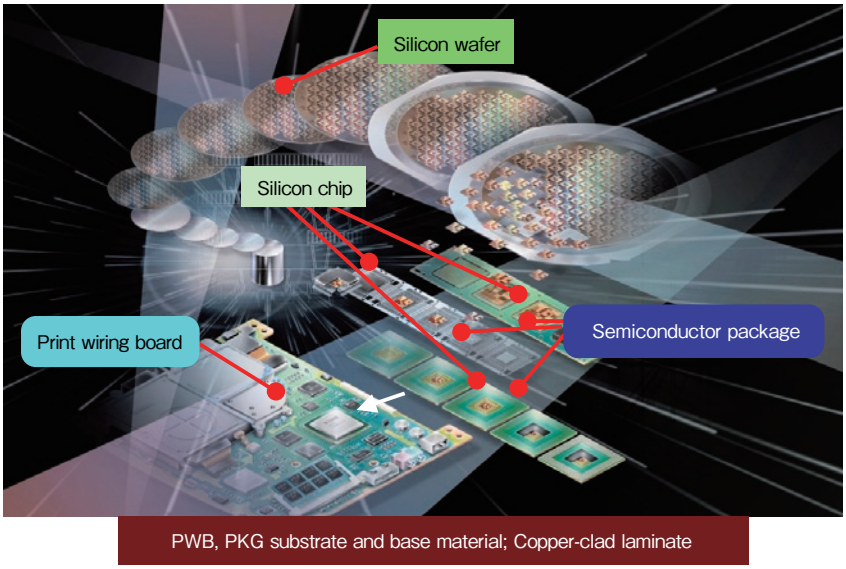

Figure 1 Hierarchical Structure of Silicon Chips, Semiconductor Package Substrates and Printed Wiring Boards

Copper-clad laminate

Photosensitive dry film

Solder resist

Figure 2 Printed Wiring Board Materials

3 Evolution of PWB

PWB was mainly developed in the United States during the 1950s. The etched foil method featuring chemical etching of copper foil on the substrate to formulate a circuit was mainly used for manufacturing PWB. In Japan, the first prototype paper phenol copper-clad laminate was manufactured in 1954, and about half a century later, technology has evolved into mass production of cutting-edge PKG substrates equipped with high Tg epoxy copper-clad laminates. These materials consist of a combination of a matrix layer of thermoset resin and basic material, and the structure is basically the same.

Circuits are wired onto these copper-clad laminates using a photosensitive dry film to produce PWB, which is classified according to the concept of "generation" depending on the materials and structures[1]. **Table 1** lists the generations and associated materials. Due to evolution, PKG substrates are much denser than PWB, and a method known as a semi-additive process (SAP) is mainly used for formulating circuitry.

Table 1 PWB and PKG Substrate Generations, Respective Materials and Substrate Structures

Generation	1st	2nd	3rd	4th		
	1955～	1960～	1975～	1995～	1993～	1997～
Copper-clad laminate	FR-1	FR-4	FR-4	FR-4	FR-4, BT	High Tg FR-4 resin
Resin	Phenol	Epoxy			Multifunctional epoxy, BT	
Base material	Paper	Glass Cloth				
Printed wiring board	Single-sided	Double-sided	Multi-layer	Build-up	Multi-layer	Build-up
Wiring density (L/S)(μm)	250/250	200/200	200/200	100/100	30/30	15/15→10/10
Application	PWB				PKG substrate	

5th generation (2005 -); Component embedded PWB, 6th generation (2010 -); Electric and optic substrate

4 Evolution of Packaging Technology

Semiconductor PKGs for electronic equipment have grown with the development of packaging technologies required for higher density (with more pins), smaller and thinner chips. **Figure 3** shows the trends of semiconductor PKGs. A DIP (Dual In-line Package) was used for pin insertion packages, in which lead pins are inserted into the through-hole of the PWB and welded, by the first half of the 1970s. Subsequently, the QFP (Quad Flat Package), using solder reflow on the components mounted on the lands of the PWB, has become mainstream to meet the requirement for narrower pin pitch. In the meantime, FC-BGA (Flip Chip-Ball Grid Array) was proposed to deal with the increased number of pins for the logic semiconductor PKGs used in micro processing units (MPUs) as IO terminals and control signal terminals increased. This method, formulating solder ball at the back of PKG for area array packaging, has been widely used for major electronic equipment as a driving force for narrowing pitches and PKG miniaturization.

Ceramic PKG substrates were the main logic semiconductor PKG substrate, but the development of highly temperature-resistant copper-clad laminates and build-up wiring technology made organic PKG substrates available in around 1993 to meet the following three requirements:

1) Faster and higher clock frequencies
2) Fine-pitch wiring formation
3) Low costs

The low permittivity of organic materials facilitates the high-speed response in signal transmission. Accordingly, the MPU for computers is mounted on an organic FC-PKG substrate. Organic PKG substrates will continue to be developed as mainstream in future.

The recent rapid dissemination of smartphones and other mobile electronic terminals reflect the demand for faster, thinner and smaller products which are more compact and power-efficient. To meet these requirements, the SiP (System in a Package) technique is proposed, which integrates several semiconductor devices into a single PKG. A notable advance is achieved, particularly in 3D packing technique, for stacking different semiconductor PKGs and semiconductor chips.

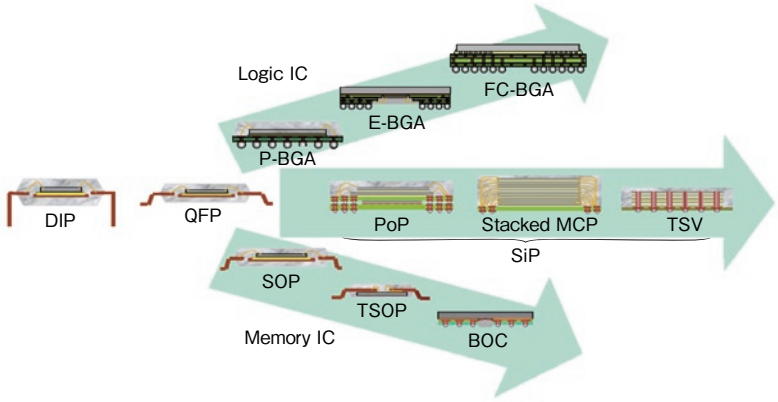

Figure 3 Trends of Semiconductor Packages

5 Issues and Development Trends of the FC-PKG Substrate

In addition to FC-BGA for MPUs, the FC-CSP (Chip Scale Package) is used for application processors. The FC-PKG substrate has some issues to be studied such as micro wiring formation, reductions in warp to meet the requirements for shrinking and multi-bump semiconductors.

5.1 Fine-Pitch Wiring Formation

The fine-pitch wring formation on PKG substrates is also an important issue to achieve high-speed processing of semiconductor chips. In the most advanced PKG substrate, Line/Space (L/S) = 10/10 μm was attained. The fine-pitch wiring forming method is a SAP method using plating technique. Here, a circuit is formed on the inter-layer materials (build-up materials) on the film, while laser-beam machining using CO_2, etc. is used for the inter-layer connection of materials. A micro through-hole of less than 80 μm is formulated between the layers, and copper plated to connect the upper and lower layers. In future, a pitch smaller than L/S = 5/5 μm (in 2015) and L/S = 3/3 μm (in 2017) are expected. To achieve these pitches, materials with good resolution, adhesion and development are required. **Figure 4** shows L/S = 5/5 μm dry film formation. Commercialization in this area has been steadily promoted.

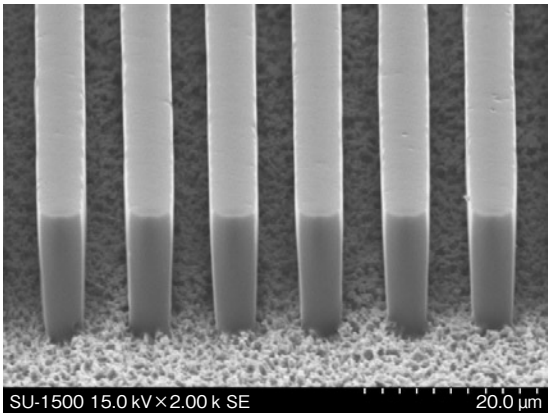

Figure 4 L/S=5/5 μm Dry Film Formation

5.2 Warp

The coefficient of thermal expansion (CTE) of silicon chips is 3 to 5 ppm/K, much lower than that of PKG substrates (16 to 19 ppm/K). The difference in their CTE is a big issue because of the production of a warp[2]. The semiconductor chip and PKG substrate are usually connected with a metal. Lead-free solder melts at 260 ˚C to connect the bump on the chip and the copper bump on the PKG. During the subsequent cooling process, however, the substrate shrinks more than the chip due to the difference in their CTE, causing a warp. If the warp of the PKG substrate is marked, the reliability of the secondary connection with the motherboard may be lost. To solve this problem, the CTE of the PKG substrate must be decreased, namely approximated to the CTE of the silicon chip. The PoP FC-CSP market will demand 0 ppm/K for the CTE of the base materials in 2015 to 2017.

6 Future Trends of PKG Substrates and Material Design Technology

As described in Section 4, 3D PKGs will be popular in future. Typical semiconductor PKGs using 3D packaging technology include PoP for stacking logic and memory ICs, MCP (stacked Multi-Chip Package) for staking multiple semiconductor chips, and CoC (Chip on Chip) for connecting two semiconductor chips directly.

A 3D packaging technology for stacking semiconductor chips, on which a through silicone via (TSV) is formulated, has been increasingly investigated for its potential as the next generation high-density packaging technique. As an example of these future technologies, a material design technology for PoP will be presented in this section.

6.1 PoP Trends and Technical Issues[3]

The typical PoP stacks the memory PKG on the logic PKG, and is widely used for mobile information terminals such as smartphones. The flip-chip type FBGA (Fine-Pitch Ball Grid Array) is used for the lower PKG. The pitch will narrow and the PoP shrink in future.

Materials (core materials, build-up materials, solder resists) have become thinner according to the requirements for structural components, i.e. chips and PKG substrates, and narrower inter-PKG gaps[4]. To meet these requirements, the over-mold type PKG structure shown in **Figure 5** was recently proposed[5].

Changes in the PKG structure suggest issues to be tackled, such as increased PKG warp, connection reliability, reduced impact resistance, reflow resistance, and decreased cooling performance. The subsequent section introduces an example of reducing PKG warp and improving the reflow resistance of an over-mold type thin FBGA used in the lower PoP.

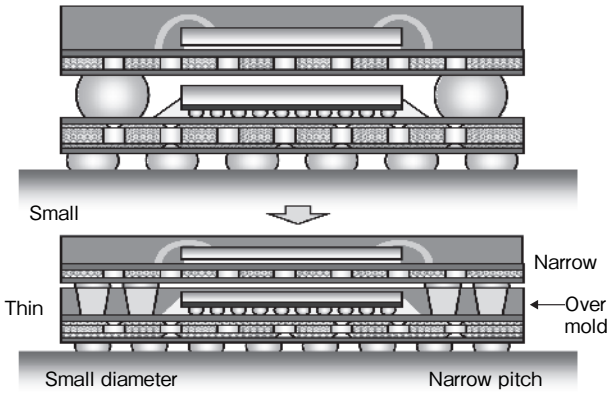

Figure 5 High-density 3D Semiconductor Package

6.2 Reducing PKG Warp and Improving Reflow Resistance

The FBGA is separated after semiconductor chips are mounted on the substrate and the substrate is encapsulated. **Figure 6** shows the external appearance of the PKG substrate with a typical post-encapsulation specification (pre-optimization). The substrate has already warped significantly at this stage, which may result in a fixed warp after separation, and significantly affect the conveyance and solder ball mounting processes.

Noting the core material and encapsulating material, which occupy a high percentage of volume in the substrate, the effect of material properties on the PKG warp was investigated using the analysis model in **Figure 7**.

First, the effect of properties of the core material on the PKG warp pre-encapsulation was analyzed, with the result shown in **Figure 8**. The PKG warp largely depends on the CTE of the core material compared with the modulus of elasticity, and lowering the core material CTE may reduce the warp.

Second, the effect of properties of the encapsulating material on the PKG warp post-encapsulation was analyzed. **Figure 9** shows the result. The PKG warp after encapsulation largely depends on the CTE of the encapsulating material compared with the modulus of elasticity, and unlike the core material, CTE optimization is required. For example, about 10 ppm/K is the optimum value in **Figure 9**.

To verify these analytical results, the warp and reflow resistance of the PKG pre- and post-encapsulation were evaluated by combining core and encapsulating materials with different CTEs. The result is shown in **Figure 10** and **Table 2**, showing good

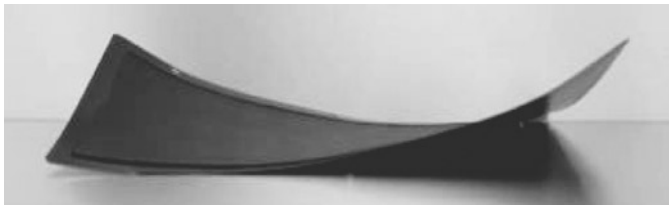

Figure 6 Example of thin FBGA post-encapsulation (pre-optimization)
Package size: 14×14×0.51 mm, Chip size: 8×8×0.12 mm
Substrate thickness PKG: 270 μm,
Thickness of core substrate: 100 μm,
Thickness of encapsulation: 240 μm

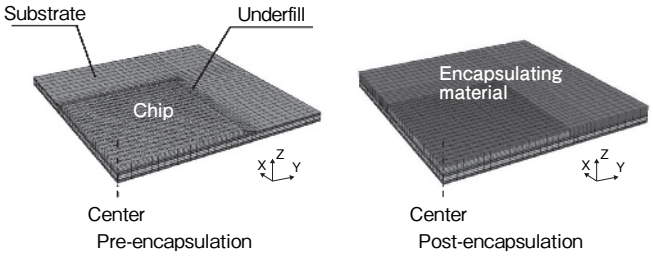

Figure 7 Package Warpage Analysis Model

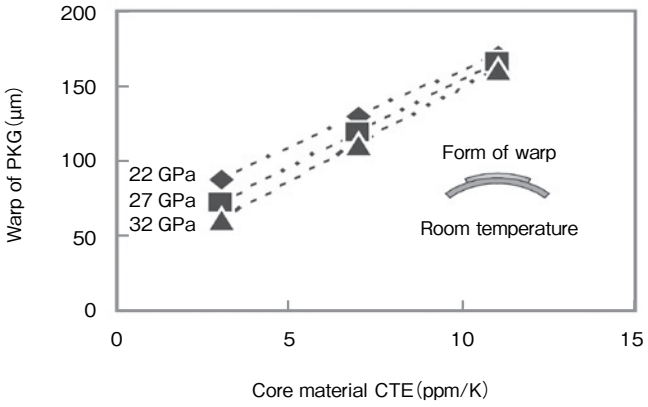

Figure 8 Influence of Substrate Material Property on Package Warpage

agreement between the analytical and experimental results. However, the pre- and post-encapsulation warps were not observed in material system No. 4, consisting of a core material with a small CTE and an encapsulating material with an optimized CTE respectively. **Figure 11** shows an example of post-encapsulation warp (after optimization), which was largely reduced compared with that of pre-optimization (**Figure 6**).

To analyze the high-temperature reflow resistance, encapsulating materials with low moisture absorption and effective adhesion (Nos. 3 and 4) suppressed the interfacial delamination, and improved reflow resistance.

Based on these results, combining the core material with a low CTE and encapsulating material with high adhesion and optimized CTE could reduce the pre- and post-encapsulation PKG warp, and improve the reflow resistance.

Structural components and materials other than the mentioned core and encapsulating materials (build-up materials, solder resist, underfill materials) have been analyzed as required to investigate the suitability of these components and materials in terms of the warp on PKG and reliability.

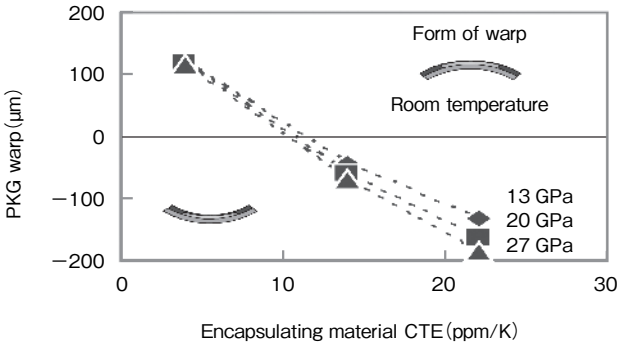

Figure 9 Influence of Encapsulation Material Property on Package Warpage

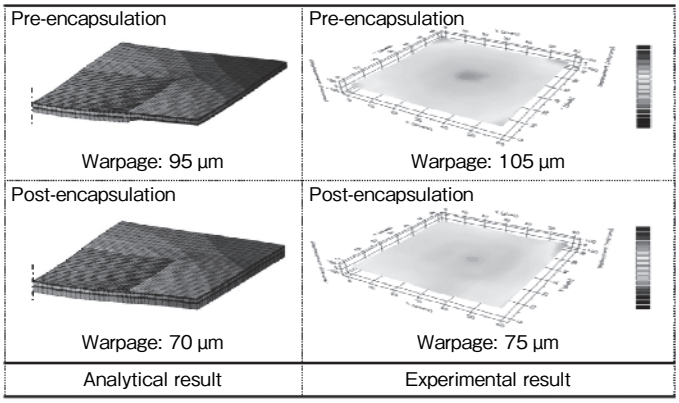

Figure 10 Comparison of Package Warpage Analysis and Experimental Results

Table 2 Package Evaluation Result

Material system		No. 1	No. 2	No. 3	No. 4
Core material	CTE (ppm/K)	9	3	3	3
Encapsulating material	CTE (ppm/K)	20	20	14	7
	Moisture absorptivity * (%)	0.5	0.5	0.3	0.2
	Adhesion with chips * (MPa)	0.1	0.1	0.9	1.0
PKG warp (μm)	Pre-encapsulation	180	105	105	105
	Post-encapsulation	85	135	120	75
Reflow resistance (defect rate)	Moisture absorption level 3	0/6	0/6	0/6	0/6
	Moisture absorption level 2	1/6	4/6	0/6	0/6
	Moisture absorption level 1	6/6	6/6	0/6	0/6

* Moisture absorption level 1

7 Changes in PKG Material Improvement Technologies and Unlimited Advance in Technology

In addition to improvements in epoxy resin for increasing Tg and decreasing the CTE in PKG substrates, various methods, including increases in the volume of inorganic filler to substrate materials have been discussed and their effectiveness presented[6]. The CTE lower than Tg is 80 ppm/K in the current epoxy resin. Submicron (about 500 nm) silica particles with smaller CTE (0.5 ppm/K) are generally processed with surface treatment by silane[7]. To further decrease the CTE when high-density filling of silica particles reaches the limit, a technology for the molecular design of resin with a higher-order structure has been applied, making 2.8 ppm/K available. To decrease the CTE to below 0 ppm/K, the molecular design of organic materials and a means of controlling silica filler volume are important.

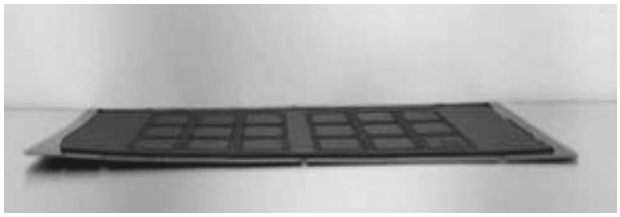

Figure 11 Example of Thin FBGA Post-encapsulation (post-optimization)

3D packaging technology is expected to be widely used in future in various areas such as mobile information terminals as electronics advance further. Combined with MEMS and optical packaging technology, system integration in various areas will be accelerated.

Packaging technology is key to achieving these targets, and the packaging materials supporting such technology must meet diversified and complex requirements. This means ever-greater importance of design and development encompassing multi-functionality.

8 Future Vision Focusing on Business 20 Years Out

Electronics technology will continue to progress as the base technology in various industries, including electronic equipment, automobile, medical equipment and robot. Its application and the form of end products will drastically change. This report traced the history of material technology over the past half-century. While end products have changed from televisions to computers and smartphones, material technology used for PWB and PKG substrates has developed based on the resin technology for matrix layers. Looking ahead two decades, the development of materials is still based on chemistry, and the following technologies may be required for developing materials:

1) Polymer synthesis technology based on molecular design
2) Interface control technology in molecular units (nanoparticles)
3) Bonding technology for organic, inorganic and metal materials, and hybrid materials made of different types of materials
4) Development of signal transmission technology (combination of electric and optical technologies)
5) Super-fine photosensitivity technology

In addition, with a lineup of packaging materials, Hitachi Chemical will strive to improve its material system solution (MSS) (**Figure 12**) that synchronizes the properties of materials, structural design, packaging and reliability evaluation by developing materials to create highly functional packaging materials and contribute to the development of society.

Figure 12 MSS of Package Substrate and Package Materials

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