Semiconductor Wafer Process Materials

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The shrinking design rules, increased number of layers, and application of new materials are the aspects characterizing progress in semiconductor devices, in accordance with the downsizing and multi-functionalization of electronic devices such as smartphones, tablet computers, notebook PCs, and so on. The required properties for semiconductor wafer process materials have been increased and diversified under these circumstances.

Hitachi Chemical has been developing and commercializing various kinds of CMP (Chemical Mechanical Polishing) slurries, "HS-series", wafer coating materials such as siloxane-based spin-on film, "HSG", and low temperature curable organic type photo-definable dielectrics, "AH-series" suitable for stress buffers and the redistribution of bumps. Technical trends, features of our products and future works for CMP slurries and wafer coating materials are described in this report.

1 Introduction

Recently, efforts to downsize and functionally expand electronic devices, typically cell phones and personal digital assistants, have been rapidly promoted. Semiconductor LSIs are getting denser under these circumstances, therefore shrinkage of its design rule and multilayer metallization (Logic ICs currently have ten or more layers, for example) are the key technologies. Planarization of each layer is essential to achieve multi-layer wiring, and application of CMP for global planarization (complete planarization) from local planarization using SOG (Spin-on Glass, Hitachi Chemical product name "HSG-R7") allows a significant reduction in step height in wiring layers. Currently, CMP is applied to a wide range of semiconductor production processes[1)], including formation of shallow trench isolation (STI), p-Si plugs, tungsten plugs, Cu wiring and planarization of interlayer dielectrics between wiring layers, and so on. At the same time, wafer-level packaging has also been accelerated in semiconductor packages to facilitate downsizing and density growth[2)]. This has expanded the applicable range of wafer coating materials such as protection films for solder bumps, and redistribution insulation layers if the redistribution of bumps is required, in addition to the conventional application of interlayer dielectrics between wiring layers and stress buffers for semiconductor packages. The trends in CMP slurry, and wafer coating material technology, the present state of development and future deployment are presented in this report.

2 CMP Slurries

2.1 STI Slurries

STI process is polishing the area in contact with transistors is most sensitive to defects among CMP processes. Therefore, preventing polishing scratches is particularly important as shown in **Figure 1**. **Figure 2** suggests that as the wiring of semiconductor devices shrinks, even the small scratches would seriously impair the operation of devices. High planarity performance in the STI process is essential since STI is the bottom layer of the device as well as reducing scratches.

Slurries using silica (silicon oxide) abrasive have been widely used in the STI CMP process, but silica slurries also have issues such as scratches, insufficient planarity and low removal rate. Focusing on cerium oxide ("ceria") particles, which have advantages such as less scratches and high removal rate, Hitachi Chemical developed submicron ceria slurries in the HS-8005 series, featuring less scratches and high removal rate of SiO_2 film, which was marketed in 1999. We also developed the HS-8102GP additive, primarily composed of organic polymers for ceria particles, and marketed at the same time. This additive is absorbed in SiO_2 film to facilitate the polishing of uneven surfaces, and stops polishing when the SiN film, which is the polishing stop film in the STI process, is exposed.

Table 1 shows the HS-8005 series lineup. To reduce scratches, Hitachi Chemical has developed various products with optimized particle sizes and distributions. With the HS-8005-X3, polishing scratches can be reduced to 1/10 or less of the HS-8005. We established production technology for fine control of particle size and distribution of ceria particles to supply stable quality products, with top global shares of the ceria slurry market. To meet the requirements for further scratch reduction, Hitachi Chemical developed ultra-fine particles in the form of the NC series, for next-generation slurry. While conventional ceria particles are crushed for microparticulation, the size of NC series particles is mud by crystalline growth method, minimizing scratches due to large size particles. **Figure 3** shows the appearance of the HS-NC and HS-8005. HS-NC is an ultra-fine, transparent, nano-level particle.

The functions of additives include to control the removal rate of the polishing stop film (SiN, pSi) and planarity of the SiO_2 film. To improve these functions, we designed new organic polymers to develop new additives (HS-7000 series) to control and optimize the planarity performance of additives to the film to be polished (SiO_2, SiN, pSi). The 7000GP series provides higher adsorption by specially controlling the adsorption to the SiO_2 film. Polishing scratches caused by the aggregation of particles were also reduced by controlling the adsorption to ceria particles. Hitachi Chemical has offered various combinations of ceria slurries and additives to meet the various needs of customers.

Recently, ceria slurries have been increasingly used in the ILD (Interlayer Dielectric) and PMD (Pre Metal Dielectric) CMP process in place of silica slurries. We have also striven to develop ceria slurries with much higher removal rate of SiO_2 as required in these CMP Processes.

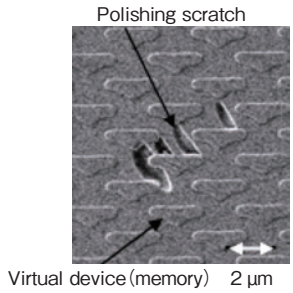

Figure 1 SEM Image of Scratch on STI Test Pattern Wafer

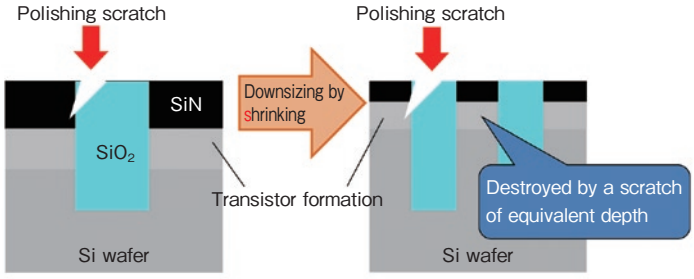

Figure 2 Influence of Scratch to the fine Design-rule Device

Table 1 Polishing Performance of Ceria slurries with Additive

Slurry	HS-8005	HS-8005-X	HS-8005-X2	HS-8005-X3	HS-NC
Removal rate [nm/min]					
SiO_2 film	350	330	300	250	250
SiN film	8	8	8	8	4
pSi film	1	1	1	1	<1
Planarity* [nm]	<10	<10	<10	<10	<10
Scratch [relative value]	100	40	20	<10	<1

＊Dishing of Active/Trench=100/100 μm
Polisher：Rotary type
Polishing pad：Polyurethane hard pad

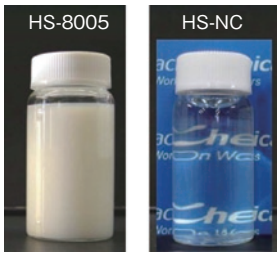

Figure 3 Appearance of HS-8005 and HS-NC

2.2 Metal Slurries

Low-resistance Cu wiring has recently been replacing Al wiring to improve the operating speed of semiconductor devices, and Cu-CMP is essential for the Cu wiring manufacturing process. In Cu-CMP, two types of slurries are used for two-step polishing processes, the process of removing Cu and the process of removing the underlying barrier metal (Ta, TaN). High removal rate, high planarity and high Cu:Ta selectivity are required for Cu-CMP, while a low defectivity and high planarity (controllable selectivity of Cu: Ta: SiO_2) are required for barrier metal CMP.

Table 2 shows the CMP performance of the HS-H700 for Cu and the HS-T915 for barrier metal developed by Hitachi Chemical. When polishing Cu using the HS-H700, a complex layer is formed on the Cu surface due to the chemical reaction of the complexing agent included in the slurry, and the complex layer is removed by the friction between the polishing pad and wafer surface at a removal rate of more than 500 nm/min. The mechanism achieving planarity of less than 50 nm (dishing) is selective polishing of the complex layer only on the protruding portions, and the polishing pad does not remove the concave portions to protect the surface. Since there is a trade-off between removal rate and planarity, the choice of chemical composition and an abrasive coating for polishing are key techniques for optimizing both variables. The wiring yield for advanced devices of 1X -2X nm generations is affected by several nanometers of Cu corrosion (voids) or defects slurries providing high-process stability in mass production processes are also required.

Barrier metal CMP removes three materials, Cu, Ta and SiO_2, simultaneously. Since a mechanical action is more effective for removing Ta and SiO_2 compared with Cu, the choice of abrasive is important. Excessive mechanical strength causes scratches and even fine scratches may result in wiring open and short failure. We have succeeded in minimizing defects by adding a small quantity of soft colloidal silica for the abrasives. As residual insoluble Cu complex on the polished surface has recently become an issue, Hitachi Chemical has developed slurries that hardly produce any residue or are easily removed in the post-CMP cleaning process. **Figure 4** shows the result of defect evaluation on the wafer after CMP with HS-T915. Compared with conventional

Hitachi Chemical slurries, a significant reduction in defects is obvious in newly developed slurries.

Figure 5 shows a cross-sectional TEM photo of a patterned wafer polished with Cu slurry HS-H700 and barrier metal slurry HS-T915. The two-step polishing process, using two different slurries, achieves highly flat Cu wiring with fewer defects. Because the ultimate goals for the dishing amount of a 100 μm wide wiring pattern is less than 10 nm and for the erosion amount in dense narrow wiring under several nanometers (**Table 2**), steps produced in Cu-CMP is recovered by controlling the polishing selectivity in barrier metal CMP. The finishing would be optimally planarized when the selectivity of Cu:Ta:SiO_2 is in the order of 1:3:3 under optimized polishing conditions and oxidizer concentration. Although there are various patterns in devices, such as logic, memory and image sensor, adjustments are required according to customers' needs.

Table 2 CMP Performance of Metal Slurry

Metal slurry			HS-H700 series	HS-T915 series
Application			Cu slurry	Barrier slurry
Polishing condition (Pressure : kPa)			14.0	10.5
Removal rate (nm/min)		Cu	850	27
		TaN	<1	95
		SiO_2	—	90
		SiOC	—	31
Planarity (nm)	100/100 μm	Dishing	<50	<10*
	9/1 μm	Erosion	<10	<5*
Defect and corrosion			Good	Good
Cu residual			None	None

*HS-H700 series slurries were used for Cu-CMP
Polisher : rotary type
Polishing pad : polyurethane hard pad

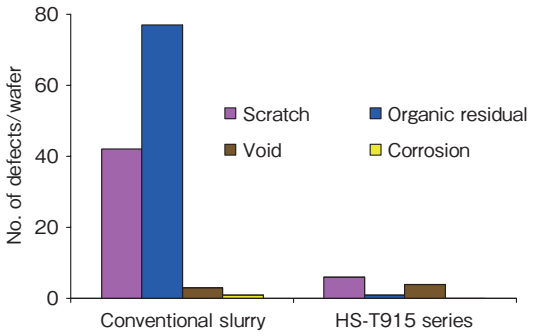

Figure 4 Defect Classification and Counts after Barrier CMP

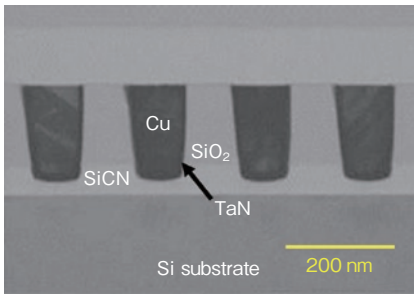

Figure 5 Cross Section of Patterned Wafer after CMP

3 Wafer Coating Materials

Hitachi Chemical and group companies have marketed coating type insulation materials such as polyimide and siloxane resins as interlayer dielectrics and wafer coating materials for semiconductors. These materials have been used in semiconductor devices. To meet the requirements of recent semiconductor packages for downsizing, high speed and high capacity and density, area-array type packagings such as BGA (Ball Grid Allay) and CSP (Chip Size/Scale Packaging) and 2.5- or 3-dimensional packagings, such as TSV (Through Silicon Via) have become increasingly prominent[2]. In these packagings, redistribution on the chip is required to adjust the design of chips and those of substrates (module boards). **Figure 6** shows a schematic illustration of an example. Hitachi Chemical promoted R&D on coating materials for photo-definable dielectrics as semiconductor insulation materials for redistribution insulation layers, etc. and marketed the AH series.

The insulation layer requires various properties, including photosensitivity to simplify engineering processes, heat resistance, mechanical and electric properties, chemical resistance and compatibility with redistribution. In addition, lower curing temperature will be required to prevent device degradation due to high-temperature processing, or when materials with low heat resistance may be used in the preceding processes[3]. The AH series will meet various needs as described before utilizing Hitachi Chemical's proprietary photosensitive materials, heat-resistant materials, resin synthesis and resin modification technologies.

Table 3 shows the general properties of an AH series material, which is made of positive photosensitive resin that can be developed with alkali solution (2.38% TMAH), and offers practical photosensitivity. Curing temperatures of 180 to 200 °C, which are lower than those for existing polyimide resins, could be achieved by optimizing chemical species and taking into account the temperatures causing a cross-linking reaction of the base resin with a cross-linker. The mechanical properties, which are by no means inferior to those for polyimide resin, could be implemented by additives which are compatible with the base resin. The low curing temperature and elastic modulus result in low residual stress, which

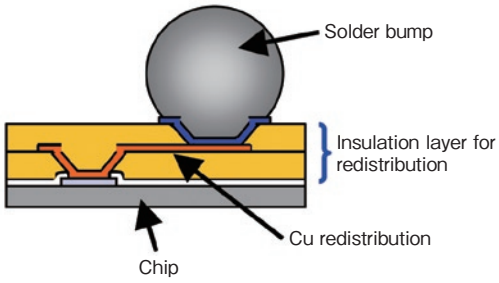

Figure 6 A Semiconductor Packaging Bearing a Redistribution Layer

Table 3 General Properties of an AH-Series

Item	Unit	AH series
Thickness	μm	2～20
Optimum exposure*	mJ/cm^2	400
Curing temperature	℃	180～200
Glass transition temperature	℃	>200
Elastic modulus	GPa	2.0
Elongation	%	50
Coefficient of thermal expansion	$10^{-6}/K$	58
Residual stress	MPa	20

＊Film thickness after curing 10 μm

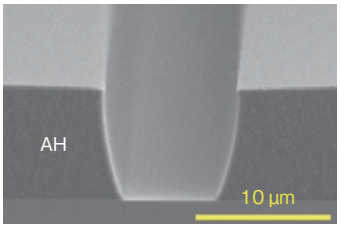

Figure 7 A Cross Section of a Cured AH Pattern

allows the material to be used as insulation layers for the chip stack packages, on which the warpage of the silicon substrate is an issue. **Figure 7** shows the cross-section of a cured AH pattern. Although this figure shows a rectangular pattern, one with smoother profile is feasible by optimizing the cure conditions. This makes it possible for the AH series to be applied to various packages, possessing through via, and bump connection. A wafer-level CSP was prepared using the AH series to investigate its reliability. The result showed that moisture/reflow resistance and thermal cycle resistance are both very good[4].

As explained above, the AH series have good photolithographic performance and their physical properties and reliability remain good even after cure at relatively low temperatures such as 200 °C. For this reason, the AH series are applicable to novel semiconductor packages which have recently come to the fore.

4 Conclusion

This report described the technical trend and status of development in CMP slurries for STI, Cu wiring and wafer coating materials as those used in semiconductor wafer processes.

Electronics will evolve into ubiquitous and cloud entities in future, which requires finer, more sophisticated and power-efficient semiconductor devices and smaller, faster and denser semiconductor packages. Under these circumstances, applications of new materials for next-generation semiconductor devices have been well discussed. For example, the use of insulating oxide layers with good filling performance for the STI process in place of TEOS and HDP-SiO_2, and the application of interlayer dielectrics with lower dielectric constant for the ILD process have been promoted. Changing barrier metal from Ta to Ru and Co has been accelerated in metal processes due to the advantage of the latter for filling performance of Cu into micro trenches. CNT (carbon nanotube) has been studied for wiring instead of conventional Cu. The application of three-dimensionalizing techniques such as TSV (Through Silicon Via) and PoP (Package on Package) is also subject to considerable discussion[2]. Moreover, semiconductor packages will become increasingly diversified, and MEMS[5] and flexible devices[6] may grow as well.

Based on the above technical trends, the application of the CMP process has also increased, and in addition to the properties required for CMP slurries such as a low defectivity rate and high planarity, the development of new slurries to suit changes in target materials to be polished is also important. As for wafer coating materials, improvement of properties for not only insulation, resolution, and residual stress, but also reliability are important.

Semiconductor electronics will evolve continually. We will go on proposing new wafer process materials by accurately predicting future technical trend of cutting-edge devices.

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