Techniques for Analyzing Underfill Materials for Semiconductor Packages

Naoya Suzuki
New Business Development Headquarters
Tsukuba Research Laboratory

1 Summary

Semiconductor packages tend to be miniaturized and thinner. In parallel, problems such as increasing warpage of package and/or lowering reliability of interconnection become severe. Therefore, it is important to predict warpage of packages and strain loaded at soldar bumps accurately and to implement these predictions in the material design. In this work, focusing on underfill materials for FC-BGA, we simulated and evaluated the influence of material properties on the warpage and reliability. We also report the improvement of the accuracy in the analysis of warpage and strain.

2 Features of Technology

- Package warpage can be predicted precisely by considering the viscoelastic behavior of the underfill material.
- The life of bumps can be predicted by investigating the relationship between the evaluation of interconnection reliability and the bump strain analysis.

3 History of Research

The structure of FC-BGA is shown in **Figure 1**. FC-BGA is composed of numerous materials of different roles. As the chip size and the bump pitch are becoming larger and finer, respectively, the problems such as increasing warpage and/or lowering reliablity in interconnection have been exposed. Also, the gap between the chip and the substrate is getting narrower due to the finer bump pitch. Therefore, filling the gap with the underfill material without voids becomes difficult. Under these circumstances, the early-stage proposal by precise evaluations and simulations is demanded.

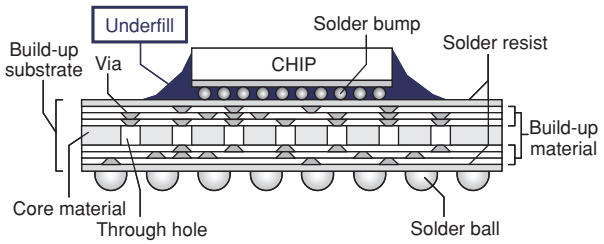

Figure 1 Structure of FC-BGA

To simulate warpage and strain more precisely, we analyzed the effect of underfill materials on FC-BGA and studied the results of TEG evaluation.

4 Content of Technology

(1) Methods of Evaluation and Analysis

Figure 2 shows the FC-BGA used in warpage evaluation and thermal cycle test. Specifications of the FC-BGA are shown in **Table 1**.

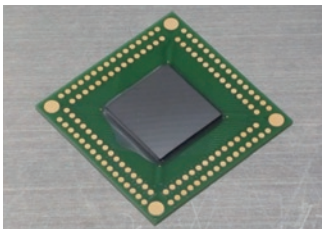

Figure 2 Overview of FC-BGA for evaluation

Table 1 Specifications of FC-BGA for evaluation

Item	Specification
Chip size	20.0×20.0×0.8 mm
Bump pitch	150 μm pitch area array
Bump count	16900 bumps
Substrate size	45.0×45.0×0.9 mm
Underfill	CEL-C-3730S
Core material	E-700G(R)
Solder resist	SR7300G

The simulation model for FEM (Finite Element Method) analysis is shown in **Figure 3**. Package warpage and bump strain during thermal cycling were analyzed using this model. **Figure 4** shows the viscoelastic properties of the underfill material that were input into the simulation. The master curve was obtained from the results of viscoelasticity measurements at different frequencies.

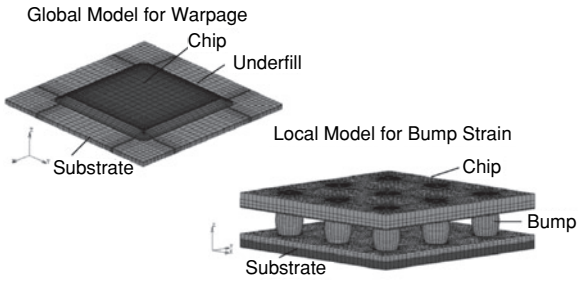

Figure 3 Simulation model for FEM analysis

(2) Result of Investigation

Figure 5 shows a comparison of evaluation and simulation of warpage. The simulation carried out with viscoelasticity coincides precisely with the actual warpage measured at each temperature. This indicates that considering the viscoelastic behavior of the underfill material is effective in precise analysis of package warpage. **Figure 6** shows an example of bump strain simulation during thermal cycle test. Bump strain tends to become higher at the chip edge area. We investigated the relationship between bump strain and interconnection reliability at the chip edge area. The results are shown in **Figure 7**. Interconnection reliability is improved as bump strain decreases. This relationship suggests that it is possible to predict the lifetime of bumps precisely.

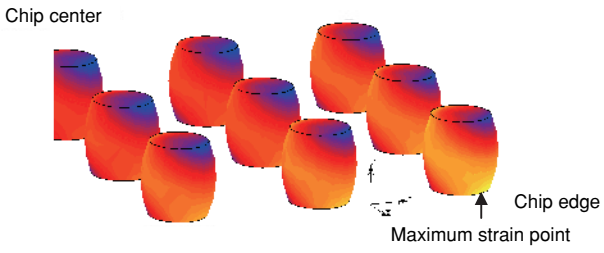

Figure 6 Illustration of bump strain simulation

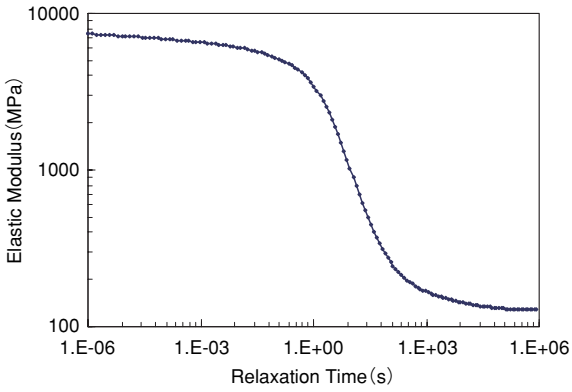

Figure 4 Underfill property imported to simulation

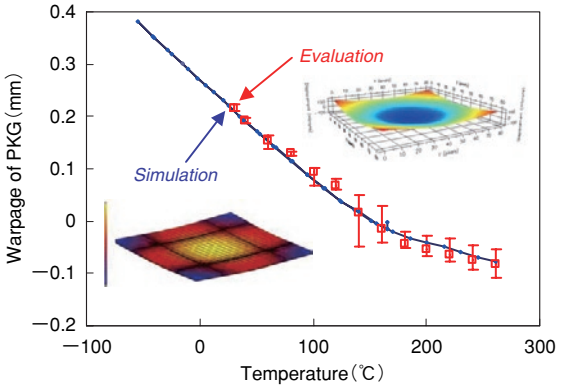

Figure 5 Comparison of warpage with simulation and evaluation

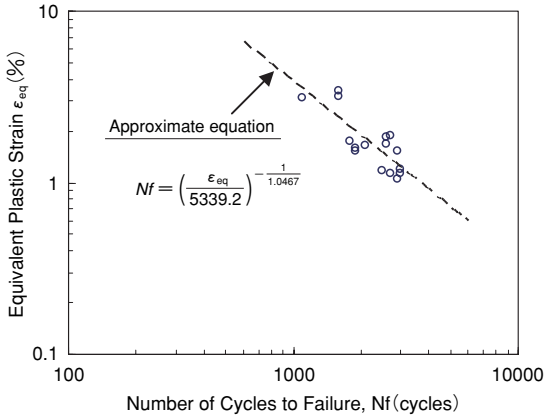

Figure 7 Relationship between bump strain and reliability

In the future, we will utilize these evaluation and simulation technologies to design the improved the reliability of materials used in wafer process and assembly process. We are also planning to create methodology for evaluating and simulating stress and fluidity of resin.

5 Future Developments

- Promoting MSS (Material System Solution) for semiconductor packages.
- Create evaluation and analytic methodology for stress and fluidity of resin.

【References】

1) Murakami, Kenkichi: Basic Theory of Rheology, pp. 151-161 (2008)
2) Lau, John H.: Flip Chip Technologies, pp. 26-61 (1998)